Examination: Introduction to Microsystems Packaging,

MKM105, 2019/2020

Date: 2020-01-17

Examination time: 14:00-18:00,
Place: "SB"-salar

Allowed tools: approved calculator and dictionary between mother language and English

Examiner: Prof. Johan Liu 070 569 38 21
Assistant Prof. Yifeng Fu 070 443 87 84

Visits to the examination room by Andreas Nylander (070 - 608 7385)

Read this first:

The maximum number of points that you can get is given after each question. A total of 60 points can be obtained for this examination.

The following scale is valid for the different grades: 3≥ 40% (24 points), 4≥ 60% (36 points), 5≥ 80% (48 points).

Block 1. (9p) General

a) Why is electronics packaging important? Explain the four main important functions of packaging. (2p)

interconnections, power, protection, thermal management, mechanical connection

b) Briefly explain the meaning of and the context in which the following concepts are used: DIP, ECA, I/O, Glob Top, LGA and UBM. (3p)

DIP: Dual Inline Package. ECA: Electrically conductive adhesive. I/O: Input/Output also the general term for a data connection. Glob Top: an encapsulation that protects a sensitive die and wirebonds using epoxy. LGA: Land grid array. UBM: Under bump metallization.

c) Describe the differences between PTH and SMT assembly and the equipment used. (2p)

PTH: Pin through hole components involves the use of leads on the components that are inserted into holes drilled in printed circuit boardsand soldered to pads on the opposite side. PTH are

placed on the PCB using a automated insertion mount machine and is soldered using a wave solder jig.

SMT: Surface mount technology either uses a screen printing step or a ink jet printing machine to dispense solder on the PCB. A pick and place machine will place the SMT components on the board and a reflow oven will reflow all the components simultaneously.

d) In the role as a design engineer, discuss pros and cons between a package design utilizing PTH components and SMT components (2p)

PTH components compared to SMT: are not as convenient for mass production, can't be made as small and can't be placed on both sides of the PCB. They are more reliable than their SMT counterparts once on the board.

Block 2. (9p) Flip chip, Wirebonding, TAB

a) Explain using your own words what TAB is and how the associated process works. (2p)

See lecture 2

b) Describe the different types of wire bonding and the associated techniques. Discuss advantages and disadvantages for wire bonding in general. (3p)

See lecture 2

c) Explain the flip chip assembly method and draw a solder bump attached to a chip including the UBM illustrating the typical material choices present there. (4p)

See lecture 2

Block 3. (10p) Packaging design

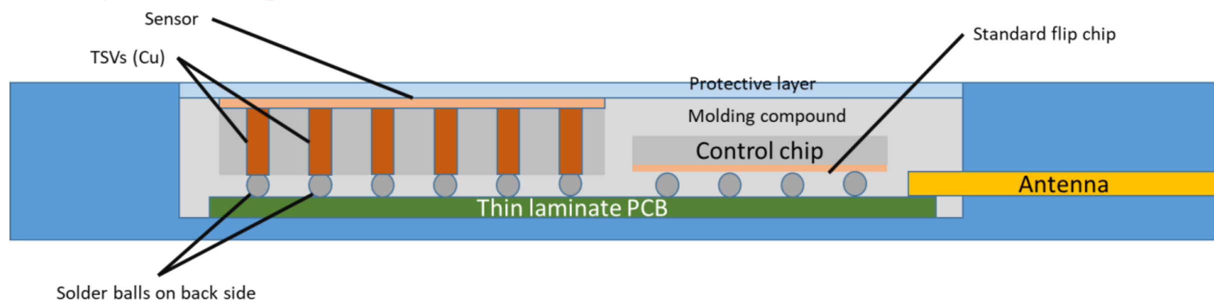
You have been tasked with the design of a biometric fingerprint reader in a credit card. The system consists of the scanner itself which is a 1.5 x 1.5 cm die whose active side will be in contact with the scanning finger through a thin (~10 μm) protective covering. The scanner has to be connected to a control chip with connections to a RFID antenna which powers the device. All of this then has to somehow be placed inside a credit card.

a) What are the packaging requirements on the system? Thoroughly describe aspects that have to be taken into account for when designing a package for this system. Think about environment, usage, cost, reliability etc. (3p)
Not too harsh environment, no extreme temperatures (should tolerate perhaps around 0 to 50°C), some moisture, very low power, easy to replace. However: Very small form factor,

especially height. Needs to be able to withstand usage and some bending every day (needs to be as flexible as a credit card is). Needs to be CHEAP.

b) Describe in as much detail as possible how you would design this system. Include material and technology choices, as well as the overall design of the system, taking into account the requirements. Include at least one schematic of the overall system. (7p)

This is just an example:



Can't do much about the flexibility, thin PCB and chips together with good molding (possibly separate underfill to prevent bubbles) might be enough. This design might be too expensive, but HUGE volumes so infrastructure costs are relatively small.

Block 4. (12p) Packaging materials and properties

a) Draw the approximate stress-strain curves for the following categories of materials: ceramics, metals, glass and polymers. For each category, briefly describe how the shape of the curve relates to the material properties elastic modulus, yield strength and ultimate tensile strength, and the real-life behavior of the material. (4p)

See picture from slides.

Ceramics: Linear steep curve up until breaking point, means that the material Is brittle and doesn't deform plastically. No yield strength, UTS is when the material breaks. High modulus

Metals: High modulus in the linear regime, has yield strength and UTS as a non-brittle material. This means metal is elastic up to a certain point, and then deforms plastically.

Glass: Similar to ceramic, but with lower modulus and UTS.

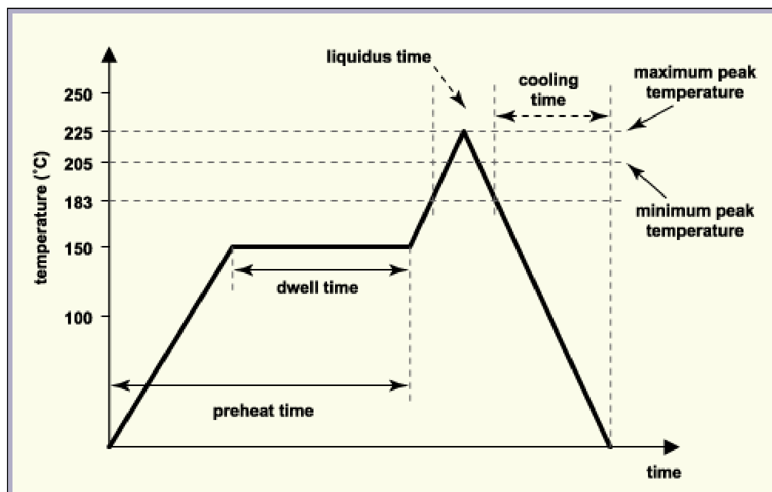
Polymers: Similar to metals, but with much lower modulus, and are able to deform much more before breaking

b) What is the glass transition temperature (Tg)? What characterizes a material that is above and below Tg? (2p)

Tg is the temperature at which an amorphous material undergoes a glass transition from glassy state (below Tg) to the rubbery state (above Tg). Several material properties change during the glass transition. In the rubbery state, materials are characterized as softer (lower elastic modulus), higher CTE, higher rate heat capacity change etc.

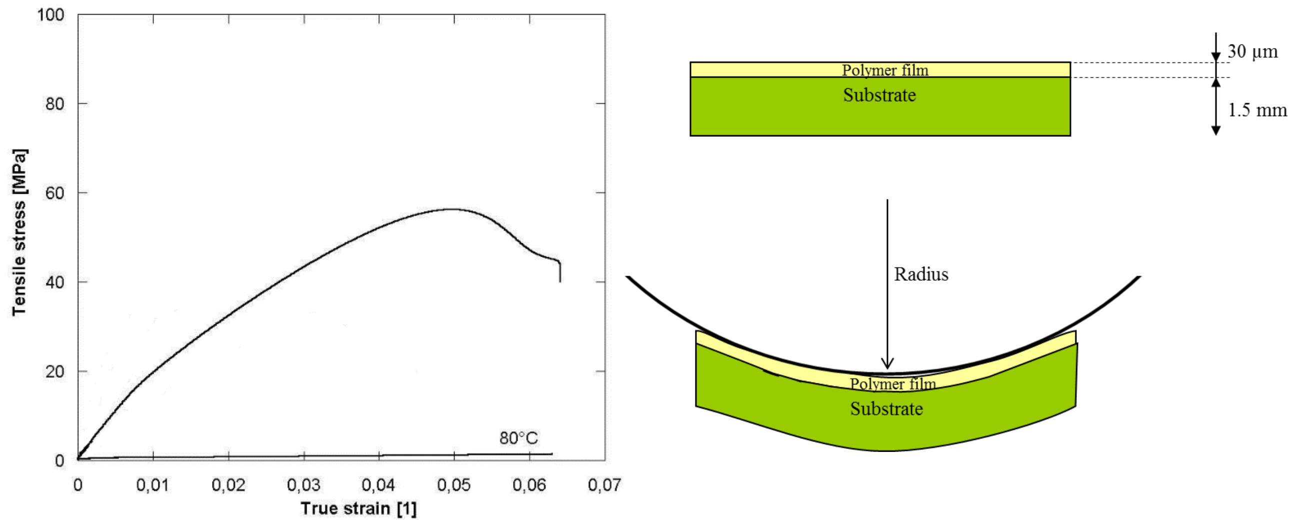
c) Draw a typical reflow profile for eutectic solder and explain the different phases of the profile. List the main components of solder and their purpose. (4p)

Solder particles – to form a solder joint
Flux – to clean surface and remove oxides during reflow
Solvent - To make the paste dispensable and the flux and solder well dispersed



Block 5. (9p) CTE

You are tasked with finding out the material properties of an unknown polymer. You deposit the polymer as a film onto a known substrate. The substrate is 1.5 mm thick, and you deposit a 30 µm thick film of the polymer. The polymer is cured at 180°C and is in a stress-free state at this temperature. After cooling down to room temperature the package bends, and you measure a curvature of 0.1 /m (equal to a radius of 10 m). The substrate has an elastic modulus of 20 GPa, a poisson ratio of 0.2 and a CTE of 20 ppm. You also make a simple tensile test of the polymer, which yields the following graph, as well as the observation that the Poisson ratio of the polymer is 0.4:



a) What is the Elastic modulus of the polymer? (1 point)

b) What is the induced stress at the substrate-polymer interface? (4 points)

c) What is the average CTE of the polymer over this temperature range? (4 points)

5a) We have a slope of approx.

$$\frac{20\,MPa}{0{,}01} = 2\,GPA$$

b) Formula: $k = \frac{\sigma_f 6(1-\nu_s) t_f}{E_s t_s^2} \Leftrightarrow \sigma_f = \frac{k E_s t_s^2}{6(1-\nu_s) t_f}$

$k = 0{,}1\ {}^1/_m \quad E_s = 20\,GPa \quad t_s = 1{,}5 \cdot 10^{-3}\,m$

$\nu_s = 0{,}2 \quad t_f = 3 \cdot 10^{-5}\,m$

$$\sigma_f = \frac{0{,}1 \cdot 20\,GPa \cdot (1{,}5 \cdot 10^{-3})^2}{6 \cdot (1-0{,}2) \cdot 3 \cdot 10^{-5}} \approx 0{,}0312\,GPa = 31{,}2\,MPa$$

c) Formula: $\sigma_f = \frac{E_f \cdot \Delta T \cdot \Delta\alpha}{(1-\nu_f)} \Leftrightarrow \Delta\alpha = \frac{\sigma_f (1-\nu_f)}{E_f \cdot \Delta T}$

$\sigma_f = 31{,}2\,MPa \quad \nu_f = 0{,}4 \quad E_f = 2\,GPa \quad \Delta T = 180 - 25 = 155\,K$

$$\Delta\alpha = \frac{31{,}2\,MPa \cdot (1-0{,}4)}{2000\,MPa \cdot 155\,K} \approx 6{,}0 \cdot 10^{-5}/K = 60\,ppm/K$$

Block 6. (11p) Thermal management

a) Leading CPU manufacturers have over the last decade shifted back and forth between using solder and paste based TIM 1 solutions in their high-end commercial products. Calculate and compare the junction temperature on the CPU side for an Intel I7 with a thermal design power (TDP) of 95 W when using thermal paste and solder-based TIM 1 solutions. The CPU generates heat on the back side of the Si chip and that all heat is transferred though the IHS up to the heat sink and CPU fan. The heatsink and CPU fan will be considered sufficiently dimensioned and will therefore hold ambient temperature on the interface to TIM 2. Assume steady state and that the heat transfer is uniformly distributed in the x-y plane. The CPU die area is 1cm^2. (5)

Using Fourier's law: $Q = \Delta T/R$

$R = (525*10^{-6}/130+50*10^{-6}/3+2700*10^{-6}/400+200*10^{-6}/3)/(10^{-2})^2 = 0.94121$ K/W

$\Delta T = T_{CPU}-T_{amb} = Q*R = 0.94121*95 = 89.41495 \rightarrow T_{CPU} = 89.41495 + 20 = 109.41°C$

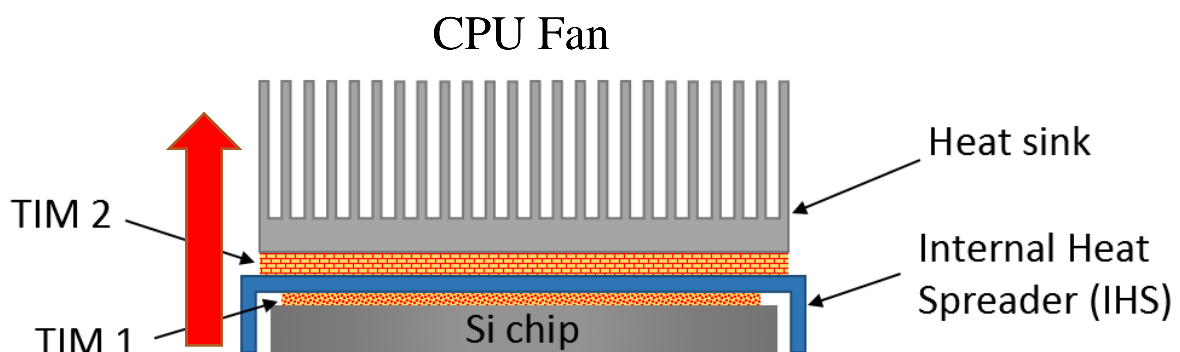
The same way for solder based TIM1

b) Discuss pros and cons when choosing between a paste and solder-based TIM 1 for use in such a commercial product from a design and reliability point of view. (2)

Paste based TIM have a much lower thermal conductivity than solder. However, solder is much more rigid and can break as a consequence to thermal stress and will in that case result in an immediate system failure. Paste is also easy to replace while solder is considered more of a "permanent solution".

c) Discuss alternative routes to lower the thermal budget without changing to solder-based TIMs and demonstrate with your own calculations the approximate impact for each of those solutions on the system found in a). (3)

Both Si chip and IHS could be thinned down for a lower R. The thermal paste could also be improved. Demonstrate by calculating what impact each of the solutions would make on the total R and speculate in the temperature impact that would make in the case when using the same system as in a)



Component	Thickness [µm]	Thermal conductivity [W/mK]
Si chip	525	130
TIM 1 (Paste)	50	3
TIM 1 (Solder)	50	81
Internal heat spreader	2700	400
TIM 2 (Paste)	200	3

Equation form:

Constants:

ε0 = Vacuum permittivity = $8.854 * 10^{-12} \left[\frac{C^2}{m^2}\right]$

Underfill processing

$$\tau_{fill} = \frac{3\mu L^2}{\sigma h \cos(\alpha)}; \qquad \tau_{fill} = \left(\frac{6\mu L^2}{(P_i - P_a)h^2}\right); \qquad \tau_p = \frac{(H_0 - f_f)}{\upsilon_p} = \frac{(H_0 - h_f)}{\dot{h}}$$

Stress, strain and life analysis

$$\sigma_f = \frac{E_f * \Delta T * \Delta\alpha}{(1 - \upsilon_f)} \qquad \sigma = k\int_{RT}^{T_g} E(\alpha_e - \alpha_s)dT$$

$$\delta = d * \Delta T * \Delta\alpha; \qquad \gamma = \frac{\delta}{h}$$

$$k = \frac{\sigma_f 6(1 - \upsilon_s)t_f}{E_s t_s^2};$$

Coffin-Manson: $\frac{\Delta\varepsilon_p}{2} = \epsilon_f'(2N)^c$

Capacitance, resistance and signal propagation

$$C = \varepsilon\frac{A}{d} = \varepsilon_0 k\frac{A}{d}; \qquad R = \rho\frac{L}{A}; \qquad v = \frac{c}{\sqrt{\varepsilon_r}}$$

Rule of mixtures

$$E = V_f * E_f + V_m * E_m = V_f * E_f + (1 - V_f)E_m$$

$$E = \frac{E_f E_m}{(1 - V_f)E_f + V_f E_m}$$