Examination: Introduction to Microsystems Packaging,

MKM105, 2017/2018

Date: 2018-01-12

Examination time: 14:00-18:00,
Place: “Maskin”-salar

Allowed tools: approved calculator and dictionary between mother language and English

Examiner: Prof. Johan Liu 070 569 38 21
Assistant Prof. Yifeng Fu 070 443 87 84

Visits to the examination room by Josef Hansson (0703-84 61 65)

Read this first:

The maximum number of points that you can get is given after each question. A total of 60 points can be obtained for this examination.

The following scale is valid for the different grades: 3≥ 40% (24 points), 4≥ 60% (36 points), 5≥ 80% (48 points).

Block 1. (10p) General

a) Why is electronics packaging important? Explain the four main important functions of packaging? (2p)
interconnections, power
protection
thermal management
mechanical connection

b) Name the main components in solder paste and their intended functions. (2p)
Solder particles – to form a solder joint
Flux – to clean surface and remove oxides during reflow
Solvent - To make the paste dispensable and the flux and solder well dispersed

c) Briefly explain the meaning of and the context in which the following concepts are used: FR-4, QFP, TSV, TIM and PTH. (3p)
FR-4: Flame Retardant 4, a glass fiber epoxy laminate for PCBs

QFP: Quad flat pack, package type with peripheral SMT leads on all 4 sides.
TSV: Through silicon via, electrical interconnections through the bulk of a chip, important for 3D-stacking of chips
TIM: Thermal Interface Material, A material placed between solid surfaces to reduce the thermal resistance between them.
PTH: Pin Through Hole, Technology for placing components on PCB, with package connections in holes through the board.

d) Define the concept "pitch". If the pitch of a single chip package is 0.4mm, and the required I/Os are 2000, estimate the size of the single chip package in the case of using BGA and QFP packages? Comment on the QFP size. (3p)
Pitch: the distance between the centers of two adjacent leads on a package. For BGA, sqrt(2000)=45 leads per side is required, giving a side of 45*0.4 = 18 mm. For QFP, 500 leads per side is required, giving a size of 500*0.4 = 200 mm, which is obviously much bigger than a package normally can be.

Block 2. (10p) Packaging Design

You have been tasked with creating a sensor system package to place on the engine of a car to monitor temperature and vibrations. The system consists of the following components:

- A control chip, which should connect to the sensors as well as the external data system of the car.
- A temperature sensor, consisting of a thermocouple (a semiconductor junction over which a voltage is measured)
- An accelerometer, consisting of a MEMS chip
- A limited (~20) number of passive components

The sensors should be placed in mechanical contact and as close as possible to the engine.

a) What are the special requirements on reliability for this system? How does the specific environment (on the engine of a car) change the reliability requirements compared to normal electronics systems? (3 points)
Being close to the engine exposes the system to extreme temperature variations and severe vibrations during operations. It can also be viewed as outside in terms of moisture and temperature when not in operation (i.e. very low temperatures as well). These electronics have to be very well shielded and protected.

b) Describe in as much detail as possible how you would design this system. Include design choices from level 1 packaging up to level 3. Specify all the materials and technologies in use at each level, with a motivation why your choice is the correct one in each case, relating to the special reliability requirements on the system. (7 points)
Multiple possible answers

Block 3. (9p) MCM

a) What is a MCM? What are the three main types of MCM substrates? Compare them in terms of manufacturing process, maximum number of layers, packaging density and manufacturing cost. (3p)
Answer:

MCM Technology	Advantages	Disadvantages
MCM-D	• Highest density • Lowest dielectric constant (2.5-4.0) • Low dissipation factor (0.001) • Controlled thermal expansion (2-3)	• High cost • Limited number of layers • Complex processing
MCM-C	• Low dissipation factor (0.001) • Controlled thermal expansion (3-7) • Maximum number of layers • Robust	• Highest dielectric constant (5-10) • Medium cost • Medium density
MCM-L	• Lower dielectric constant (3.0-4.5) • Lowest cost • Simplified processing • Robust	• High dissipation factor (0.01) • High thermal expansion (>10) • Low density

MCM-L (Laminate):
•Module based on PWB-like organic laminate substrate (typ. FR-4) using thin copper conductors, very small vias, and dense component placement.
•Based on PCBs. Glass reinforce laminates. Multiple layers for interconnecting chips
2.MCM-C (Ceramic):
•Module based on a ceramic substrate and thick-film or co-fired deposition of substrate conductor and insulating (dielectric) layers.
•Thick film or co-fired multilayer ceramic technology
3.MCM-D (Deposited):
•Module based on ceramic or silicon substrate with several thin-film layers deposited and patterned using photolithography and etching, in a process similar to IC wafer processing.
•Multilayer, thin film structures, on semiconductor or ceramic based layers, with deposited metal conductors and dielectrics

For each of the following scenarios, it has been found that the best design solution is a MCM module. Make a suggestion for which MCM substrate is best for this design choice. Clearly motivate why your choice is more suitable than the alternatives. If you don't have enough information to decide on a single one, clearly state what additional information could be used to make a final decision.

b) An accelerometer package for a communications satellite. Priority is on reliability and compactness (2p)

   Requirement on reliability in a very special system, with high vibrations at launch, harsh radiation and vacuum preventing convection cooling. However, generally uses older electronics technology, and MCM-D is too complicated and delicate. MCM-C is generally used for space applications.

b) A state of the art RF communication system. The system consists of a small number of dies, but the signal delay between them is a limiting factor. It is located in a server rack in a data center. (2p)

Relatively nice environment, but very high performance requirements suggest MCM-D

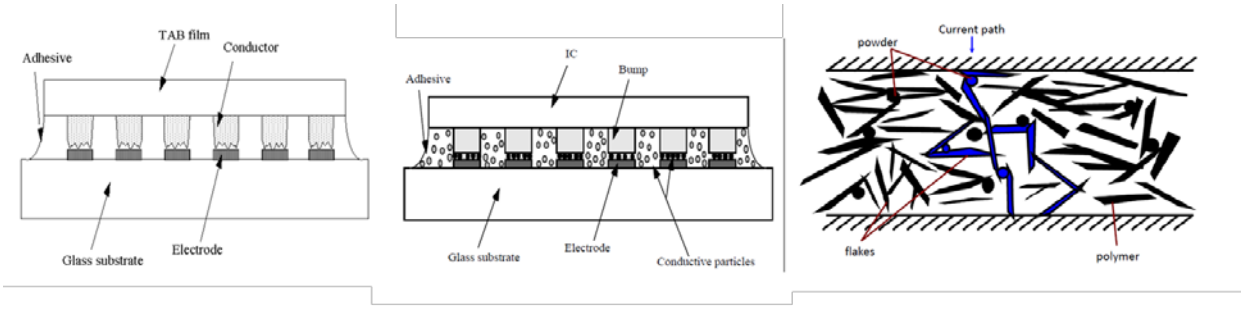
c) A mobile computing package, consisting of 3 dies with a very high number of I/Os and a high degree of connectivity between themselves, together with a significant number of passives. (2p)

Ex: High requirement on density suggests MCM-D, but a significant number of passives might be prohibitively complicated to embed in a MCM-D, so MCM-C might be a suitable compromise.

Block 4. (11p) Packaging materials and properties

a) Where and for what purpose are conductive adhesives and conductive films typically used? (2p)
For flip chip connections instead of solder. Simultaneously keeps forms attachment and electrical connection to a flip chip. In the case of ACA, also acts as underfill.

b) What are the difference between non conductive adhesive, anisotropic conductive adhesive and isotropic conductive adhesive? Use a schematic drawing to assist your answer. (4p)

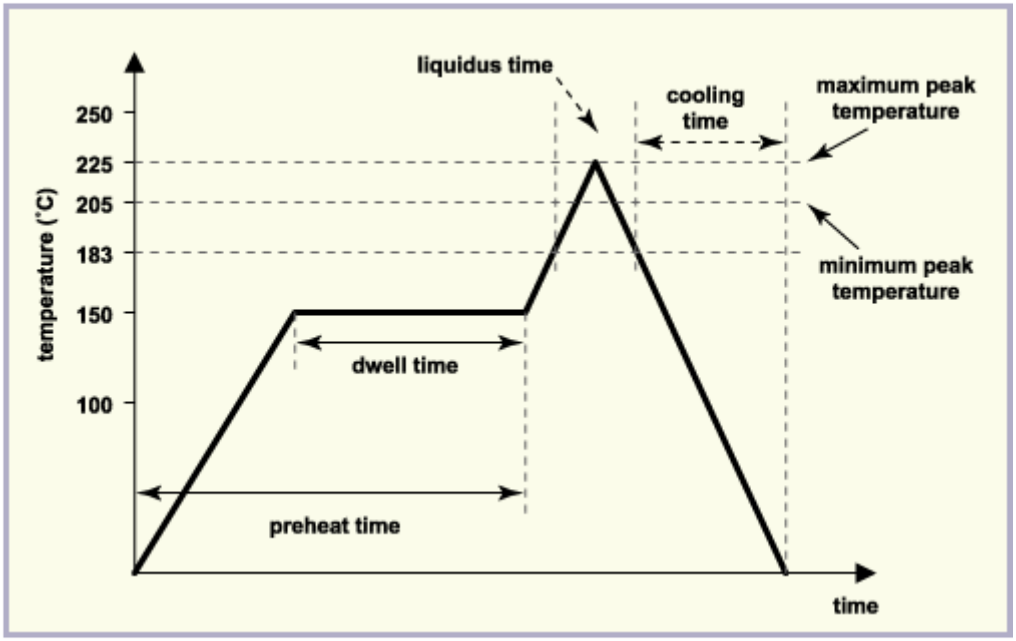


NCA
- No fillers
- Direct contact between electrodes
- Requires High pressure

ACA
- Sparse conducting fillers
- One layer of fillers between electrodes
- Requires pressure

ICA
- High concentration of conductive fillers (above percolation threshold)
- Conducts through bulk material
- Requires patterning

c) Draw a typical reflow profile for eutectic solder and explain the different phases of the profile. (3p)



d) What is the glass transition temperature (Tg)? What characterizes a material that is above and below Tg? (2p)

Tg is the temperature at which an amorphous material undergoes a glass transition from glassy state (below Tg) to the rubbery state (above Tg). Several material properties change during the glass transition. In the rubbery state, materials are characterized as softer (lower elastic modulus), higher CTE, higher rate heat capacity change etc.

Block 5. (10p) CTE, Reliability

A square flip chip die (8 mm sides, 40 μm standoff height) is soldered onto a substrate at a temperature of 180°C, at which temperature the chip and substrate are both in a stress free state. After cooling down, CTE mismatch induces stresses into the joints. The chip is made out of silicon (CTE: 3 ppm/K) and the substrate of FR-4 laminate (CTE: 14 ppm/K).

a) Assume that all of the CTE mismatch is absorbed by straining in the solder joints. Calculate the maximum strain experienced by a solder joint in the assembly. (3p)

Maximum DNP(L): corner, which is sqrt(2)*4mm=5.66mm from center.

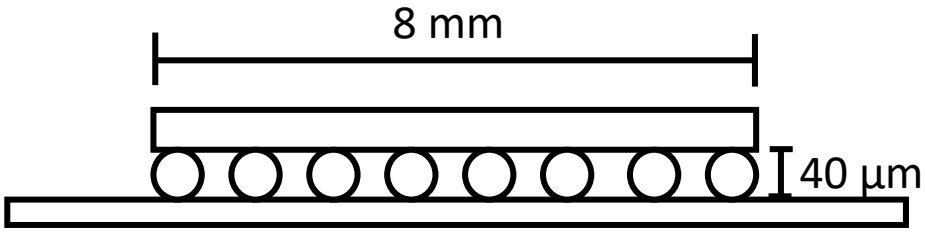
$$\gamma = \frac{L \cdot \Delta\alpha \cdot \Delta T}{h} = \frac{5.66 \cdot (14-3) \cdot 10^{-6} \cdot (180-25)}{0.04} = 0.24$$

b) Explain qualitatively what would happen to a solder joint subjected to this magnitude of strain. Would it affect the reliability, and if so, how? (3p)

At a strain of 0.24 (or 24%), all solders will have very severe plastic deformation, and might already have cracked. If not, subsequent thermal cycling will quickly induce fatigue (even if the temperature cycling only reaches a low operating temperature of 70C, that's still on the order of 0.1 in strain, with a large plastic deformation) which will lead to failure. The failure modes would be cracking or delamination depending on the strength of the solder bonding to the opposing substrates.

c) In reality, not all of the stress will be absorbed by strain in the solder joints. What other effects will the CTE mismatch induced stress have on the system, and what reliability issues could arise as consequence? (3p)
A large part of the stress will be absorbed by both die and substrate, but also by bending of the substrate (warpage). This could lead to additional reliability issues due to the now non-planar surfaces, e.g. a vertical stress component in the solder joints, or uneven connection to the rest of the system.

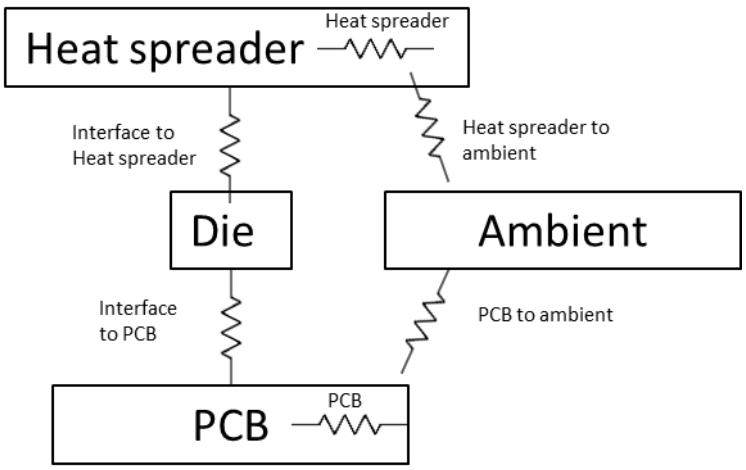
d) Describe at least two different techniques to prevent reliability issues in flip chip packages. (2p)
-Underfill is the most important component to reduce CTE related reliability issues in flip chip packages. It absorbs stress and keeps the package together.
-Chosing the right materials, both for solder and substrate (e.g. ceramic substrate instead of FR-4 to reduce the CTE mismatch, or a lower melting point solder for lower delta T)
-change dimensions: smaller packages have less problems, perhaps split up die into several. Larger standoff height also reduces strain.



Block 6. (10p) Thermal management

The manufacturer of portable electronic products has severe problems with the reliability of their latest generation of devices. The main hypothesis is that improved cooling might be a solution to the problem that is believed to have been induced by an increase in average dissipated power from 4 W to 8 W, which causes malfunction of the microprocessor chip when using the same old cooling design as before. The table below shows the thermal data for the current system, as well as two alternatives for possible improvements.

a) Based on the table below, draw a schematic picture of the system. Mark out each thermal resistance in the picture. (1 p)



b) Draw a thermal resistance diagram for the system and calculate the total effective thermal resistance for the current system (2 p)

$$R_{th} = \frac{1}{\frac{1}{4+1+3} + \frac{1}{9+10+6}} = 6.06\frac{K}{W}$$

c) What was the running temperature of the current system before the increase in power? After? (1 p) Before: $\Delta T = R_{th} * P = 4 * 6 = 24K$ After: $\Delta T = 8 * 6 = 48K$. T = 49 before and 73 after.

d) What is the maximum thermal resistance our system should have, assuming that we want the running temperature to be at least as low as before the power increase. (1 p) To get the same ΔT we need a thermal resistance of 3 K/W (8*3 = 24)

e) Argue from the data below what would be the cheapest way to ensure that the reliability issues can be "cooled" away, i.e. select whether to go for parts from the old system, from alternative A or from alternative B. You can mix and match components from each alternative. (5 points)

	Old system		**Alternative A**		**Alternative B**	
Part	Thermal resistance [K/W]	Price [a.u.]	Thermal resistance [K/W]	Price [a.u.]	Thermal resistance [K/W]	Price [a.u.]
Interface to PCB	9	1	8	2	6	4
Interface to heat-spreader	4	1	3	2	2	5
Heat spreader	1	3	0,8	4	0,2	7
PCB	10	10	8	11	3	15
PCB to ambient	6	3	4	5	2	6
Heat spreader to ambient	3	2	2	3	1	5

Equation form:

Constants:

ε_0 = Vacuum permittivity = $8.854*10^{-12}\left[\frac{C^2}{m^2}\right]$

Underfill processing

$$\tau_{fill} = \frac{3\mu L^2}{\sigma h \cos(\alpha)}; \qquad \tau_{fill} = \left(\frac{6\mu L^2}{(P_i - P_a)h^2}\right); \qquad \tau_p = \frac{(H_0 - f_f)}{\upsilon_p} = \frac{(H_0 - h_f)}{\dot{h}}$$

Stress, strain and life analysis

$$\sigma_f = \frac{E_f * \Delta T * \Delta\alpha}{(1-\upsilon_f)} \qquad \sigma = k\int_{RT}^{T_g} E(\alpha_e - \alpha_s)dT$$

$$\delta = d * \Delta T * \Delta\alpha; \qquad \gamma = \frac{\delta}{h}$$

$$k = \frac{\sigma_f 6(1-\upsilon_s)t_f}{E_s t_s^2}; \qquad \text{Coffin-Manson: } N = C(\gamma)^{\alpha}$$

Capacitance, resistance and signal propagation

$$C = \varepsilon\frac{A}{d} = \varepsilon_0 k\frac{A}{d}; \qquad R = \rho\frac{L}{A}; \qquad v = \frac{c}{\sqrt{\varepsilon_r}}$$

Rule of mixtures

$$E = V_f * E_f + V_m * E_m = V_f * E_f + (1-V_f)E_m$$

$$E = \frac{E_f E_m}{(1-V_f)E_f + V_f E_m}$$