EDA322/ DIT797: Digital Design
Exam - March 2022

Date: March 16, 2022

Time: **14:00-18:00**

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Inquiries: contact through phone, phone extension 1744

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: an A4 paper sheet (2 pages) with student notes, a calculator, are allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

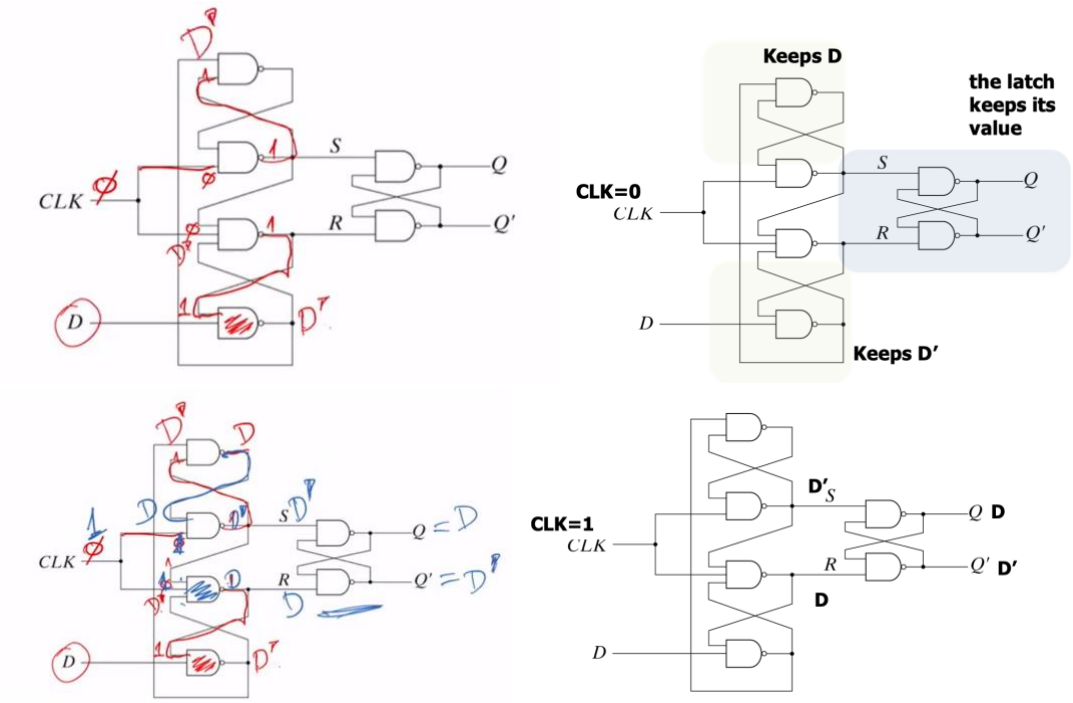
Note: *These are example answers to the exam questions for one possible set of randomized variables.*

Question 1 Arithmetic and Timing: (10 points)
Derive the Boolean function of the carry-out for a 4-bit carry-lookahead adder. Compare its delay with the Boolean function that generates the carry out of 4-bit ripple carry adder. Calculate the delay of the same paths when the adders are 8 bits. XOR: 2 ns AND/OR: 1 ns.

Answer
Similar to exercise 5 session 1.

Question 2 Sequential Circuits: (10 points)
Draw the gate-level diagram of a positive edge triggered D-flip-flop and analyze the circuit showing the values of the gate-outputs as clock switches from 0 to 1.

Answer



Question 3 Hazards: (10 points)
Minimize function $f(x_0, x_1, x_2, x_3, x_4)=\Sigma(4, 15, 17, 19, 20, 21, 23, 31)$ detect hazards and remove them.

Answer

Question 4 Number representation: (10 points)
Suppose you need to represent distance from 1 millimeter (mm) to 1 meter (m) with an accuracy of 1%.

a) Find a fixed point representation with minimum number of bits that fits the above specification.
b) Find a floating point representation with minimum number of bits that fits the above specification.
c) Which type of the above number representations is better and why?

Answer

a) 1% of a mm accuracy is 10 micrometers (μm).
This needs a resolution of 2*10 μm = 20 μm = $2*10^{-5}$ meters = 1/50000 m. If meters is the integer part we need, then we need 1 bit for integer (to count between 0-1 meters). Then, the fraction needs 16 bits to count $1/2^{16}$ = 1/64*1024) meters (which is a bit shorter than the 1/50000 meters resolution). So the fixed-point representation would require 17 bits (1.16).

Alternatively, we can count multiples of 20 μm which is the required resolution. 1 meter = 50000 * 20 μm for which we need again 16 bits (2^{16}=64K).

b) For a floating-point representation, the mantissa needs to be only 6 bits to offer accuracy of 1%. So, the resolution needs be double that: 2% = 1/50; $1/64= 1/2^6$ should then be enough (6 bits mantissa). The dynamic range is from 1mm to 1 m (10^3 mm) so it is 10^3, which is smaller than $1024 = 2^{10}$. Then, 4 bits are enough to count up to 10, so with 4-bits exponent we can represent a range of 2^{16} (which is larger than 2^{10}). With 4 bits exponent the maximum value of the exponent part is 2^{15} which is larger than the maximum value we need considering the unit is mm (10^3). The closest power of two larger than 10^3 is 2^{10}. So, we can set the bias to be 15-10 =5 so the maximum exponent to be $2^{15-5} = 2^{10}$ =1024 >1000, since the largest number to represent is 1000 mm. So, the floating point format is 6 bits mantissa and 4 bits exponent.

c) Floating point needs fewer bits than fixed point, so it is a better choice. That happens because the required accuracy is a percentage and not a fixed absolute value.

Question 5 Pipelining: (10 points)
Consider an unpipelined 8-bit Ripple Carry Adder. Consider also that the delay of a Full Adder is 100 ps, the setup time of a flipflop is 30ps and the propagation time is 20ps.

a) What is the latency, maximum operating frequency and throughput of the unpipelined version? Consider that inputs and outputs of the unpipelined version are registered.

b) Pipeline the adder to increase its throughput by 3 times. What is the latency, maximum operating frequency and throughput of the pipelined adder?

Answer
a) latency of unpipelined RCA: 8*100 +20+30= 850 ps

max operating frequency: 1/850ps = 1.18 GHz

Throughput is one addition per 850 ps = 1.18 Gops/sec

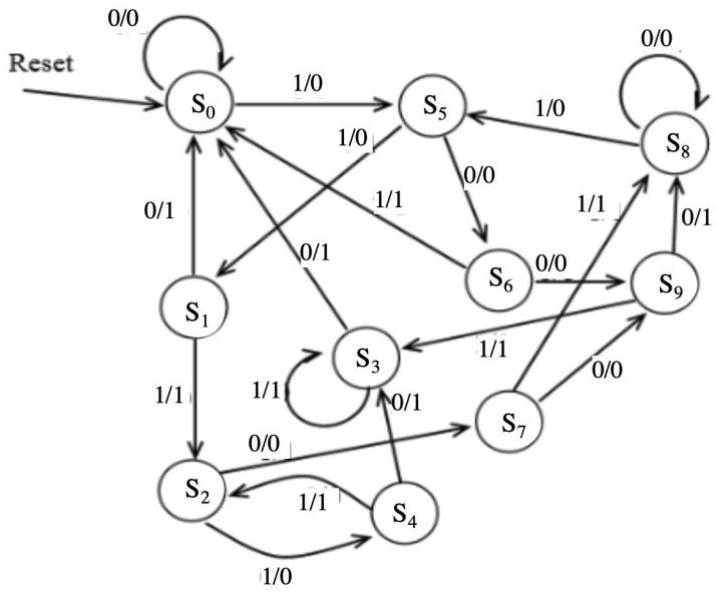
b)
In order to triple the throughput we need one results at least every 850/3 ps = 283 ps
That means we have enough time for 2 FAs (2*100 ps) plus Propagation time (20ps) + Setup time of the registers before and after the stage (250 ps in total). Adding one more FA would need 350ps which is more than what we can afford.

So in order to triple the throughput we need to split the adder in 4 stages of 2 FAs in each stage

The latency of the pipelined design would be 4*(250)ps= 1000ps= 1 ns

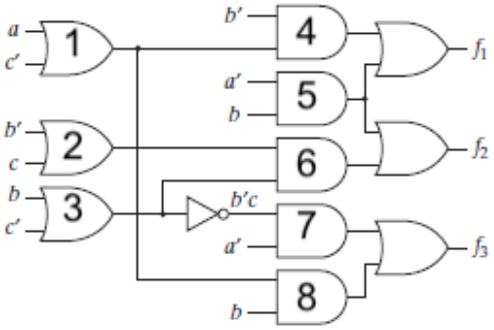
Its maximum operating frequency would be 4 GHz
And its throughput would be 1 operation every 250 ps = 4 Gops/sec

Question ~~7~~6 FSMs: (10 points)
The state diagram defines an FSM with an Input X and an output Z. The values on each arrow in the diagram have the format of X/Y.
Minimize the number of states of this FSM, list the equivalent states and draw the minimized state diagram.



Answer

Question 7 Testing: (10 points)
Activate, propagate and justify the stuck-at-0 fault at the output of the inverter.



Answer

Similar to Lecture on Testing, slides 50-54 and exercises in session 6

To activate the fault b=0, c=1 (co c'=0),
To propagate the fault a=0 (a'=1), b=0 (or a=0 and c=1) none of the inputs values we need create conflicts

Question 8 Asynchronous Sequential circuits: (10 points)
Explain (ii) what is the Fundamental Mode Restriction, and (ii) what is a Race in Asynchronous sequential circuits and when it is critical.

Answer

(i) A circuit is operating in fundamental mode if we assume/force the following restrictions on how the inputs can change (1) only one input

is allowed to change at a time, (2) The input changes only after the circuit is stable. We enforce the fundamental mode restriction to simplify the analysis of the Asynchronous circuits.

(ii) We have Races between state bits of an asynchronous sequential circuit when in a state transition more than one state bits change in a random order. This may cause the circuit to go to the wrong stable state, in which case this is a critical race.

Question 9 Memory: (10 points)
Use memory blocks that have 2^{10} entries and each entry has 1 Byte, to construct a memory of which has 2^{17} entries of 4 Bytes.
Draw the block diagram of the memory and show how the address bits are connected.

Answer
Similar to Lecture on memory, slide 23

Question 10 Reconfigurable Technologies: (10 points)
Consider the Boolean function F= a*b*c + a'*b*d + c'*d'. Map the function in the SRAM-based Lookup Tables (LUTs) of the following three FPGA devices: The first FPGA has 2-input LUTs, the second FPGA has 3-input LUTs, and the third FPGA device has 4-input LUts.

- How many LUTs are used in each FPGA device?
- How many SRAM bits in total are used in each FPGA device?
- What is the delay of the function in each FPGA device considering that (i) an SRAM cell has zero propagation delay, wires have zero delay, a 2-input AND or OR gate has a delay of 1 ns.

Answer

4-input LUTs:
- 1 LUT is needed
- 1* 2^4= 16 bits of SRAM
- The delay of the LUT is equal to an 16:1 multiplexer which needs 3 levels of 2-input AND gates and 4 levels of 2-input OR gates so its delay is 7 ns.

3-input LUTs
- 4 LUTs (in two levels)
- 4* 2^3= 24 bits of SRAM
- The delay of the 2 levels of LUT is equal to 2* 8:1 multiplexer. A 8:1 multiplexer needs 2 levels of 2-input AND gates and 3 levels of 2-input OR gates. So the total delay is 2*5 = 10 ns.

2-input LUTs
- 7 LUts (in 4 levels)

- $7 * 2^2 = 28$ bits of SRAM
- The delay of the 4 levels of LUT is equal to 4* 4:1 multiplexer. A 4:1 multiplexer needs 2 levels of 2-input AND gates and 2 levels of 2-input OR gates. So the total delay is 7*4ns = 28 ns.

END of EXAM