EDA322/ DIT797: Digital Design
Exam - June 2021

Date: June 10, 2021

Time: **14:00-18:00**

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Department: Computer Science and Engineering

Inquiries: contact through phone, phone extension 1744

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: a calculator, lecture notes, textbook, etc. are allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Note: *These are example answers to the exam questions for one possible set of randomized variables or explanations as of how a solution to an exam question can be derived.*

Question 1 Arithmetic: (10 points)
Show on a table the contents of the registers in a serial divider/multiplier at every step it takes in every iteration when it performs the operation [x]/[y] / x*y

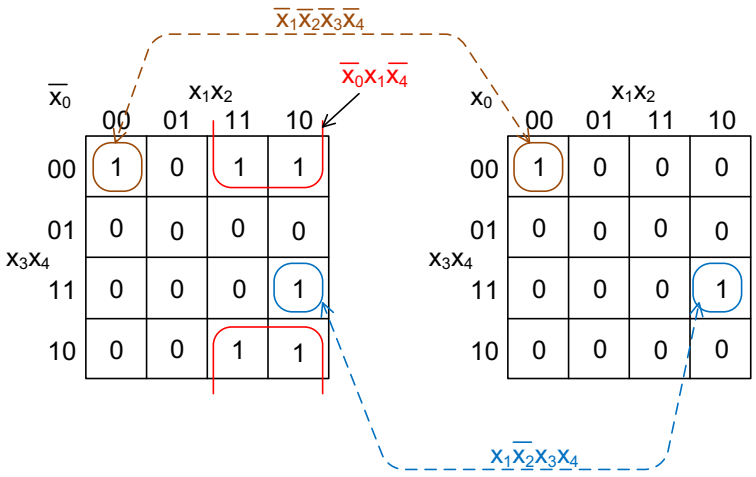
How many bits is the size of each register and how many iterations are needed?

Answer
Lecture on Arithmetic slide 11 for multiplication and slide 25 for divider. For x and y values that need 5 bits, there will be 5 iterations and the registers have to be 1 -bit wider than in the lectures.

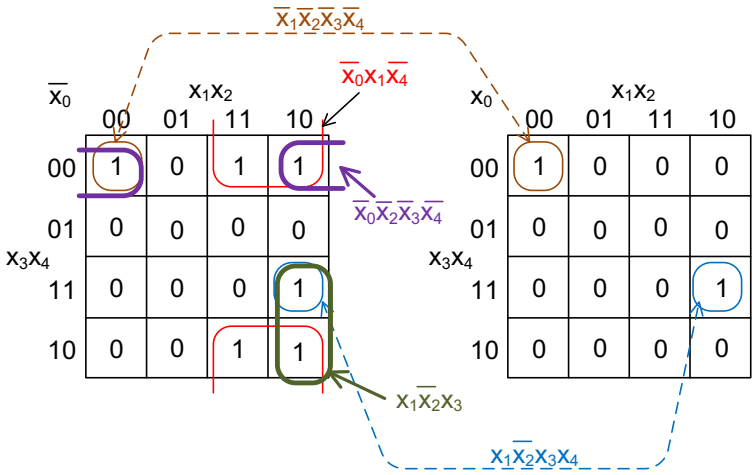
Question 2 Hazards: (10 points)

Minimize function $f(x_0, x_1, x_2, x_3, x_4,)=\Sigma(0, 8, 10, 11, 12, 14, 16, 27)$, detect hazards and remove them.

Answer



$f(x_0, x_1, x_2, x_3, x_4,)=x_1'x_2'x_3'x_4' + x_0'x_1x_4' + x_1x_2'x_3x_4$



$f(x_0, x_1, x_2, x_3, x_4,) = x_1'x_2'x_3'x_4' + x_0'x_1x_4' + x_1x_2'x_3x_4 + x_0'x_2'x_3'x_4' + x_1x_2'x_3$

Question 3 Number representation: (10 points)
Suppose you need to represent time from 1 second (sec) to 10^4 seconds with an accuracy (maximum relative error) of 5%.

Find a floating point representation that fits the above specification and uses the minimum number of bits.

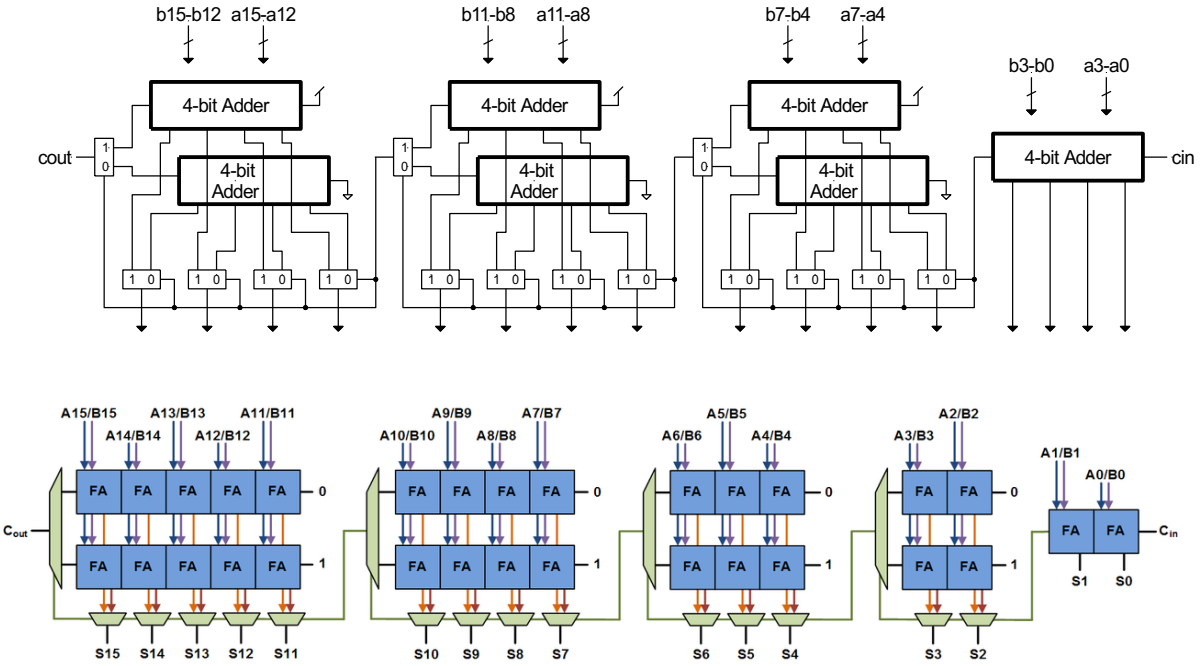
Answer
For a floating-point representation, the mantissa needs to be only 4 bits to offer accuracy of 5%. So, the resolution needs be double that: 10% = 1/10; 1/16= $1/2^4$ should then be enough (4 bits mantissa). The dynamic range is from 1 seconds to 10^4 seconds so it is 10^4, which is smaller than 16k = 2^{14}. Then, 4 bits are enough to count up to 14, so with 4-bits exponent we can represent a range of 2^{14}. We finally set the bias to 1 because we need the exponent to go up to $2^{15-1}=2^{14}$. So, the floating point format is 4 bits mantissa and 4 bits exponent, 8 bits in total.

Question 4 Pipelining: (10 points)
Consider the 16-bit Carry select adder of the figure bellow and that:

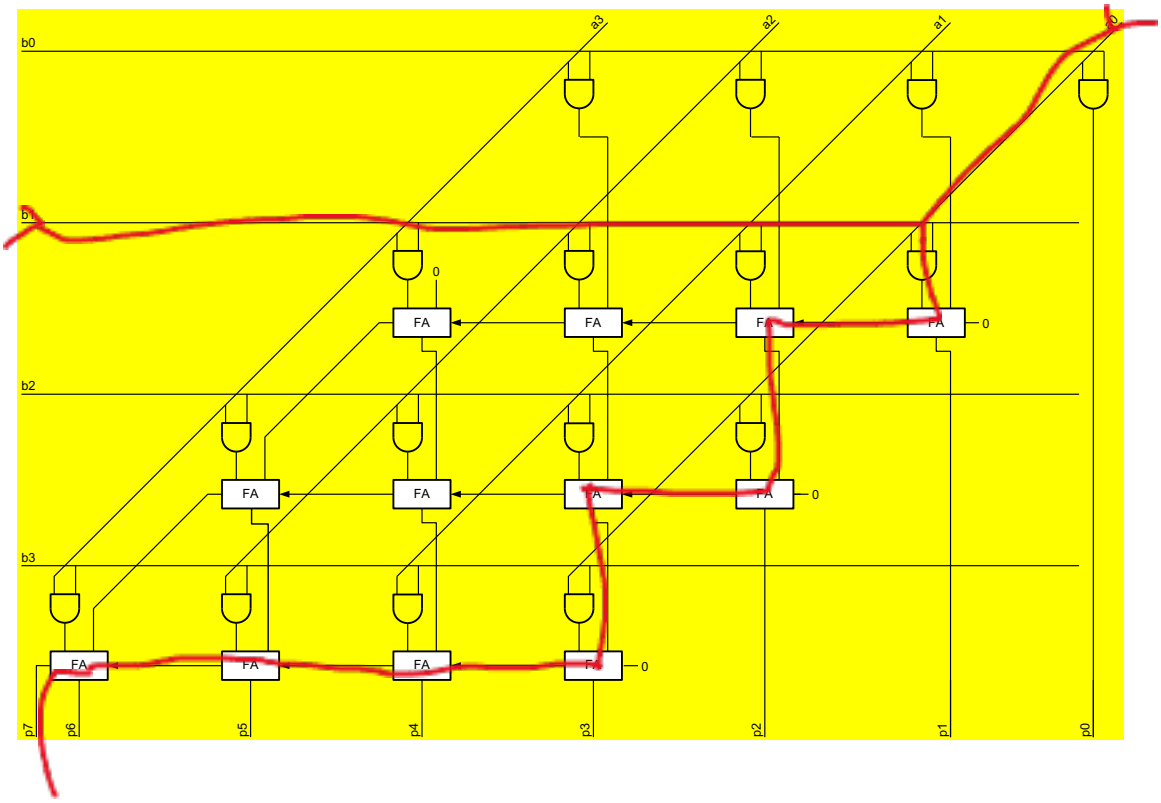
- a 2-to-1 multiplexer (from any of its input to any of its outputs) has a delay of [a] ns,
- the delay of a FA (from any of its input to any of its outputs) is [b] ns
- the inputs and outputs of the adders are registered in flip flops
- the setup time of a flip flop is [c] ns
- the propagation time of a flip flop is [d] ns

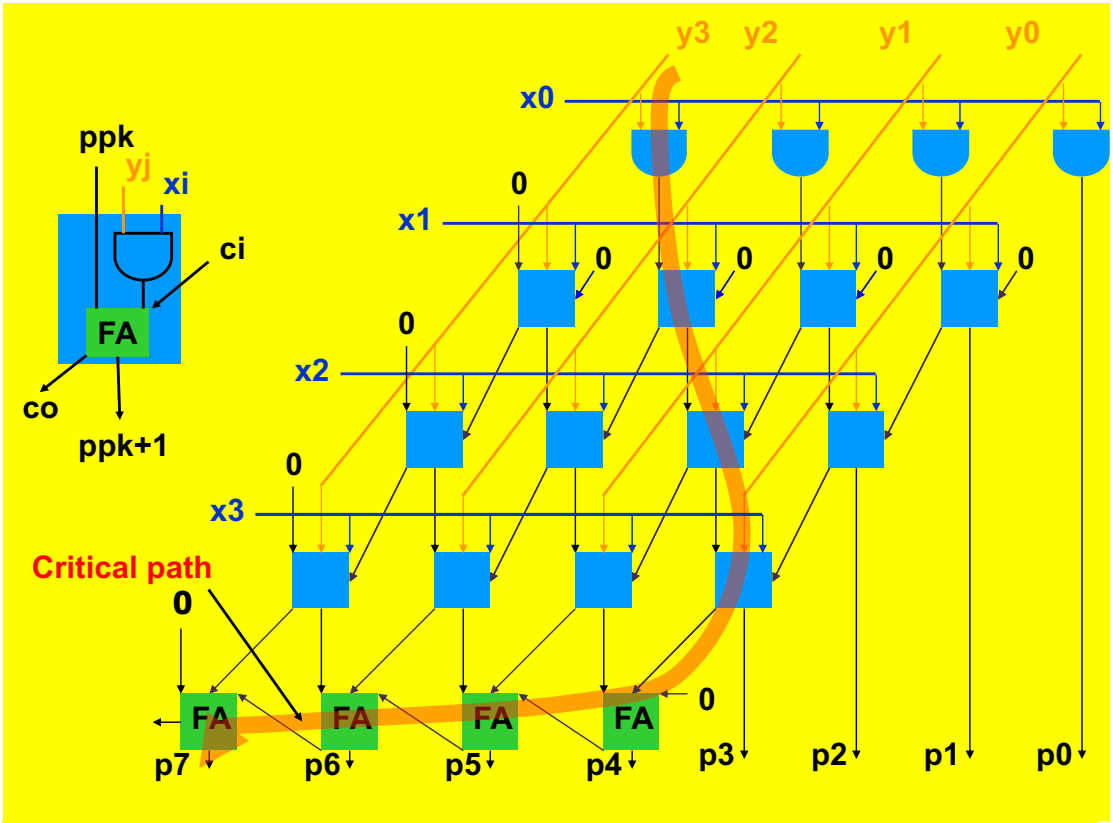
i. Show the critical path of the design and calculate its latency considering that the inputs and the outputs are registered (stored in flip flops).
ii. Calculate the throughput and maximum operating frequency of the design.
iii. pipeline the design in order for the throughput to become [e] times higher. How many pipeline stages are needed?

iv. What is the latency of the pipelined version of the design? What is its maximum operating frequency?



Answer





Above are the critical paths of the circuits used for the variations of the question.

The rest of the question can be answered similar to Exercise 2 in exercise session 7.

i) The critical path includes (1 AND + 8 FA) in the first circuit and (1 AND + 7 FA) in the second circuit as shown in the figures. It starts from an input AND, goes through the first FA to its carry out and continues to other FAs through the carry inputs and outputs until the final carry out is available next to p7. There are FFs on circuit inputs (a and b / x and y) and outputs (p). Therefore, to calculate the critical path latency, we start form the propagation delay from CLK to OUT of the input FF, followed by the logic delay, and finally the setup time of the output FF. This is the minimum time needed between two rising edges of the CLK.
Latency = d + a + 8xb + c (first circuit) or d + a + 7xb +c (second circuit)
For example assuming a =3, b =9, c =1, d =2, e =4 for the first circuit:
L = 78.
If the latency is calculated to be L ns, that is the minimum CLK period, which gives a maximum CLK frequency of 1/L GHz. It also means that we can have 1 set of results per L ns that gives a throughput of 1/L billion operations per second.

ii) To improve the throughput by a factor of e, the latency must be reduced to L/e. So we need to find a way to break the critical path into smaller parts and separate them with FFs, such that the new critical path plus the FF propagation and setup time is smaller than or equal to L/e. With the same

example values, we need to reduce L = 78/4 = 19.5 or smaller. Therefore, we can have a maximum of one FA in each stage because two FAs plus the FF delays becomes 2+18+1 > 19.5. So, in the new pipeline circuit we need to put one FF between each FA in the original critical path. That leads to 8 stages for the 8 FAs in the first circuit.

iii) The critical path in the pipelined circuit is the first stage that also includes an AND gate. So the new critical path latency is 2+3+9+1 = 15 ns. This is the minimum clock period that is equivalent to 66.6MHz maximum frequency or 66.6 M operations per second. But, the new latency is 8x15 = 120ns which is the time it takes to have the final output results, after the data has propagated through the 8 pipeline stages.

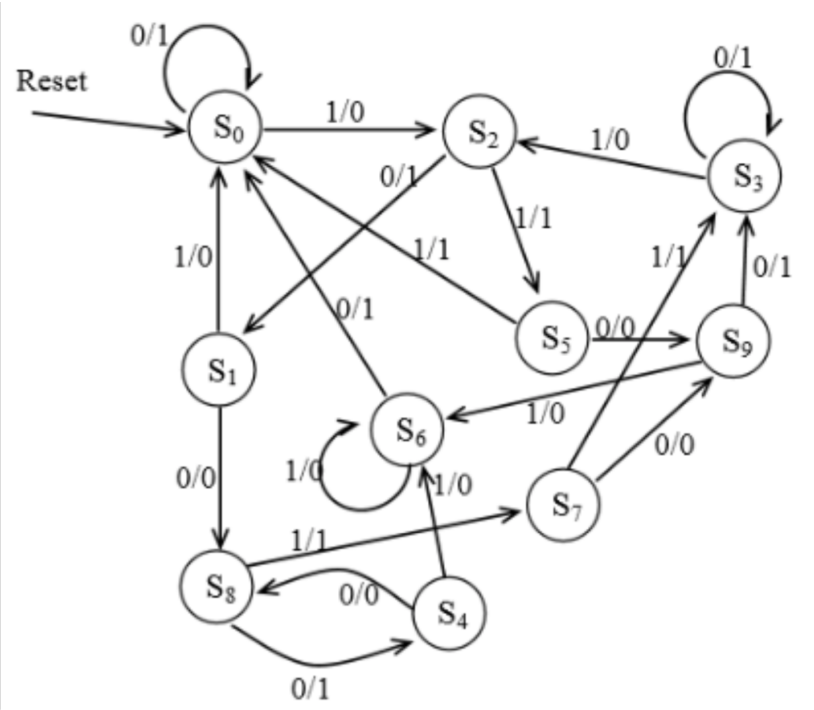
Question 5 FSMs: (10 points)

The state diagram defines an FSM with an Input X and an output Z. The values on each arrow in the diagram have the format of X/Y.

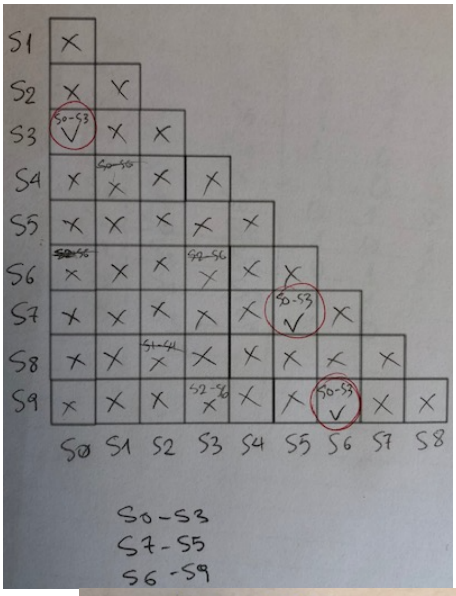
a) Minimize the number of states of this FSM and list the equivalent states.

b) Draw the state diagram and state table of the reduced FSM.

c) derive the Boolean functions for the next state bits and the output of the reduced FSM.



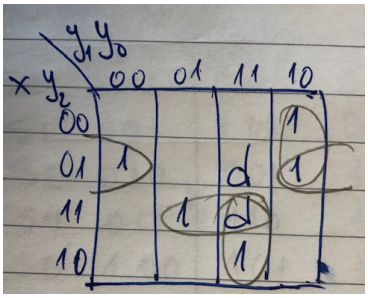
Answer



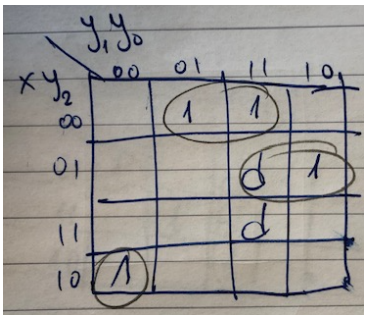
Pres.	Next State. x=0	Next State. x=1	Output x=0	Output x=1
S_0	S_8	S_2	1	0
S_1	S_8	S_0	0	0
S_2	S_1	S_5	1	1
S_3	S_3	S_2	1	0
S_4	S_8	S_6	0	0
S_5	S_9	S_0	0	1
S_6	S_0	S_6	1	0
S_7	S_9	S_3	0	1
S_8	S_4	S_7	1	1
S_9	S_3	S_6	1	0

Pres State	Next State x=0	Next State x=1	Output x=0	Output x=1
S0'	S0'	S2	1	0
S1	S8	S0'	0	0
S2	S1	S5'	1	1
S4	S8	S6'	0	0
S5'	S6'	S0'	0	1
S6'	S0'	S6'	1	0
S8	S4	S5'	1	1

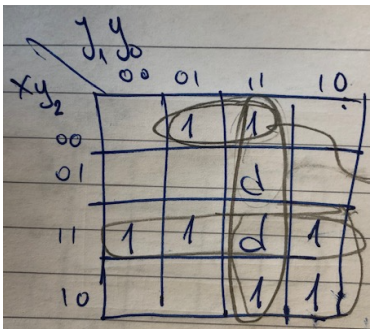
Pres. State $y_2\,y_1\,y_0$	Next State x=0 $Y_2\,Y_1\,Y_0$	Next State x=1 $Y_2\,Y_1\,Y_0$	Output(z) x=0	Output(z) x=1
S0' 000	000	010	1	0
S1 001	110	000	0	0
S2 010	001	100	1	1
S4 011	110	101	0	0
S5' 100	101	000	0	1
S6' 101	000	101	1	0
S8 110	011	100	1	1
111	d	d	d	d



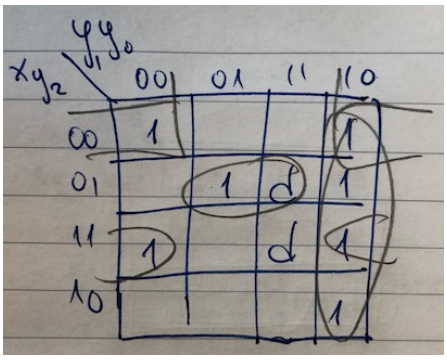
$Y0 = x'y_1\,y_0' + x'y_2\,y_0' + x\,y_2\,y_0 + x\,y_1\,y_0$



$Y1 = x\,y_2'\,y_1'\,y_0' + x'\,y_2'\,y_0 + x'\,y_2\,y_1$



$Y2 = x' y_2' y_0 + y_1 y_0 + x y_2 + x y_1$



$Z = y_1 y_0' + x' y_2' y_0' + x' y_2 y_0 + x y_2 y_0'$

Question 6 Testing: (10 points)
The cost of a chip is 10 SEK when its yield is 50%. What should be the yield in order for the cost to be 5 SEK.

Answer

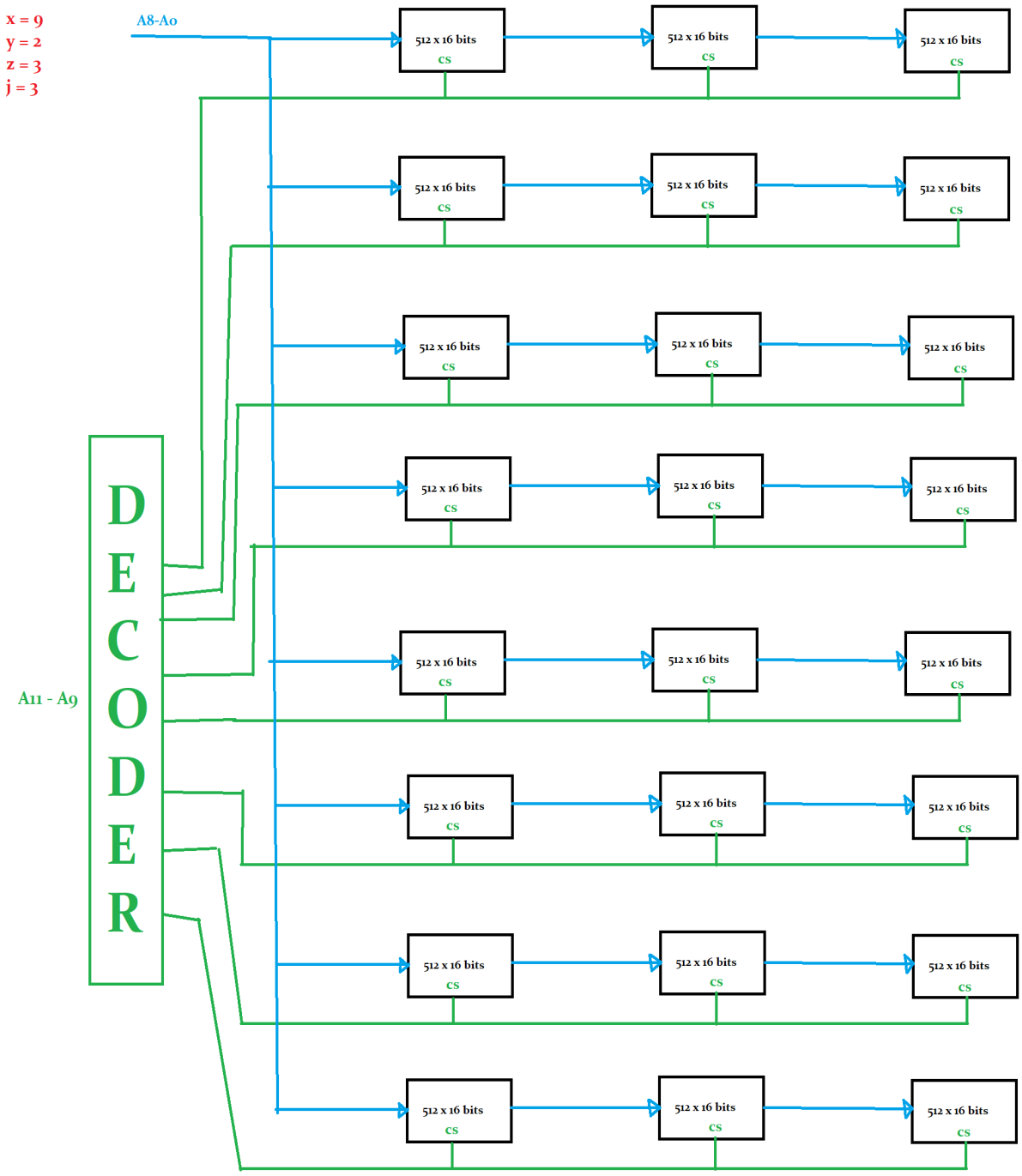
Assume a wafer has *n* chips, then

Chip cost = (wafer cost)/ (0.5* *n)* = 10 SEK

Wafer cost = 0.5**n* * 10 SEK = 5*n* SEK
For chip cost 5 SEK:
chip cost = wafer cost/(y**n*) = 5**n*/(y**n*) = 5 SEK cents ⇔
y = 5/5 = 100%

Question7 Memory: (10 points)
Use memory blocks that have $2^{[x]}$ entries and each entry has [y]Bytes, to construct a memory of which has $2^{[x+z]}$ entries and [j]*[y] Bytes per entry.
Draw the block diagram of the memory and show how the address bits are connected.

Answer
Similar to Exercise 4 in Exercise Session-6



Question 10 Power: (10 points)
Why is it important to reduce the power in an embedded/portable system (e.g., a mobile phone, vehicle electronics). Describe ways to reduce power of the digital circuits in these systems.

Why is it important to reduce the power in a high-performance computing system (e.g., a supercomputer, a data center). Describe ways to reduce power of the digital circuits in these systems.

Why is it important to reduce the power in a general purpose system (e.g., a desktop computer). Describe ways to reduce power of the digital circuits in these systems.

Answer:
Lecture on Timing, Delays and Power, slides 38-41, 47

Question 9 Sequential circuits: (10 points)

a) Describe what is the setup time, hold time and propagation time of a flip flop.
b) Consider that setup time = [x] ns, hold time = [y] ns, and propagation time =[z] ns. Explain if two cascaded flip-flops (one giving input to the other) with these timing characteristics would operate correctly, and why.
c) If they would operate correctly what would be their maximum operating frequency? Otherwise, if they would not operate correctly, explain what can happen in the second flip flop and why.
d) Consider now that hold time = [z] ns, and propagation time =[y] ns and answer (c) again.

Answer

a) Lecture on Timing Delay and power, slide 19 (also lecture on Sequential circuits slide 21)
b+c+d) check condition Tp>Th as explained in Lecture on Timing Delay and power, slide 21

If the above condition is met then clock period >Ts+Tp

If the condition is not met the second flip flop will get in a metastable state

Question 10 Reconfigurable Technologies: (10 points)
Draw the block diagram of a 3-input FPGA logic cell and show its configuration when its programmed to implement a 5-input logic **NAND** gate with registered ouput.

Answer
Lecture on Reconfigurable Hardware, slide 15, and similar to slide 18 (make truth table of NAND and load it to the 16bits of the LUT).

END of EXAM