EDA322/ DIT797: Digital Design
Exam - March 2021

Date: March 17, 2021

Time: **14:00-18:00**

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Department: Computer Science and Engineering

Inquiries: contact through phone, phone extension 1744

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: a calculator, lecture notes, textbook, etc. are allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Note: *These are example answers to the exam questions for one possible set of randomized variables or explanations as of how a solution to an exam question can be derived.*

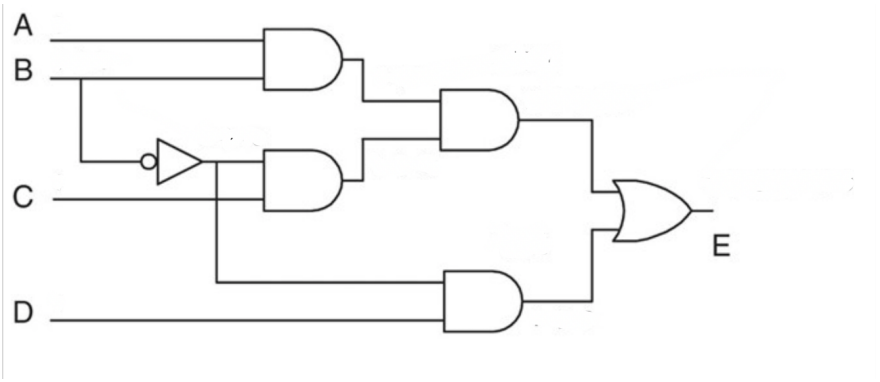
Question 1 Arithmetic: (10 points)
Show on a table the contents of the registers in a serial divider/multiplier at every step it takes in every iteration when it performs the operation [x]/[y] / x*y

How many bits is the size of each register and how many iterations are needed?

Answer
Lecture on Arithmetic slide 11 for multiplication and slide 25 for divider. For x and y values that need 5 bits, there will be 5 iterations and the registers have to be 1 -bit wider than in the lectures.

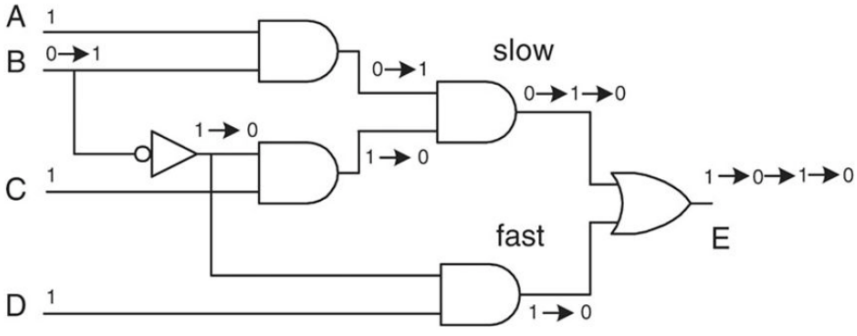
Question 2 Hazards: (10 points)

a) Show a dynamic hazard in the following circuit.
b) Draw a hazard-free version of the circuit using a NOR-based/NAND-based SR-latch.



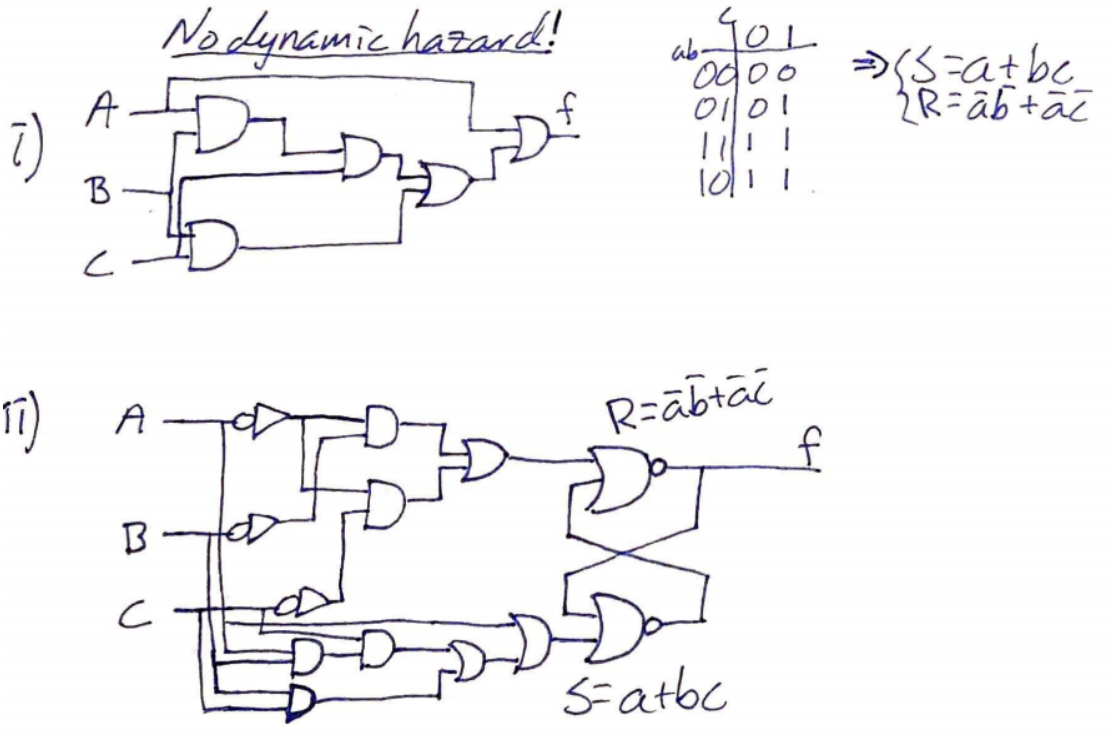
b) Draw a hazard-free equivalent of the circuit.

Answer
a)



b) similar to lecture 11 slides 78-81

Below is an example of one of the circuits that did not contain a dynamic hazard, but where we still add a NOR-based SR-latch.



Question 3 Number representation: (10 points)

Suppose you need to represent distance from 0 to 10 meters (m) with 0.5 millimeter (mm) precision (absolute error <= 0.5 mm).

Find a fixed point representation that fits the above specification.

Answer

a) 0.5 millimeters (mm) absolute error needs a resolution of 2*0.5 mm = 1 mm = 1/1000 meters.
If meters is the integer part we need, then we need 4 bits for integer (to count between 0-10 meters). Then, the fraction needs 10 bits to count $1/2^{10}$ = 1/1024 meters (which is a bit shorter than 1 mm resolution). So the fixed-point representation would require 14 bits (4.10).
Alternatively, we can count millimeters which is the required resolution. 10 meters = 10000 mm for which we need again 14 bits (2^{14}=16K).

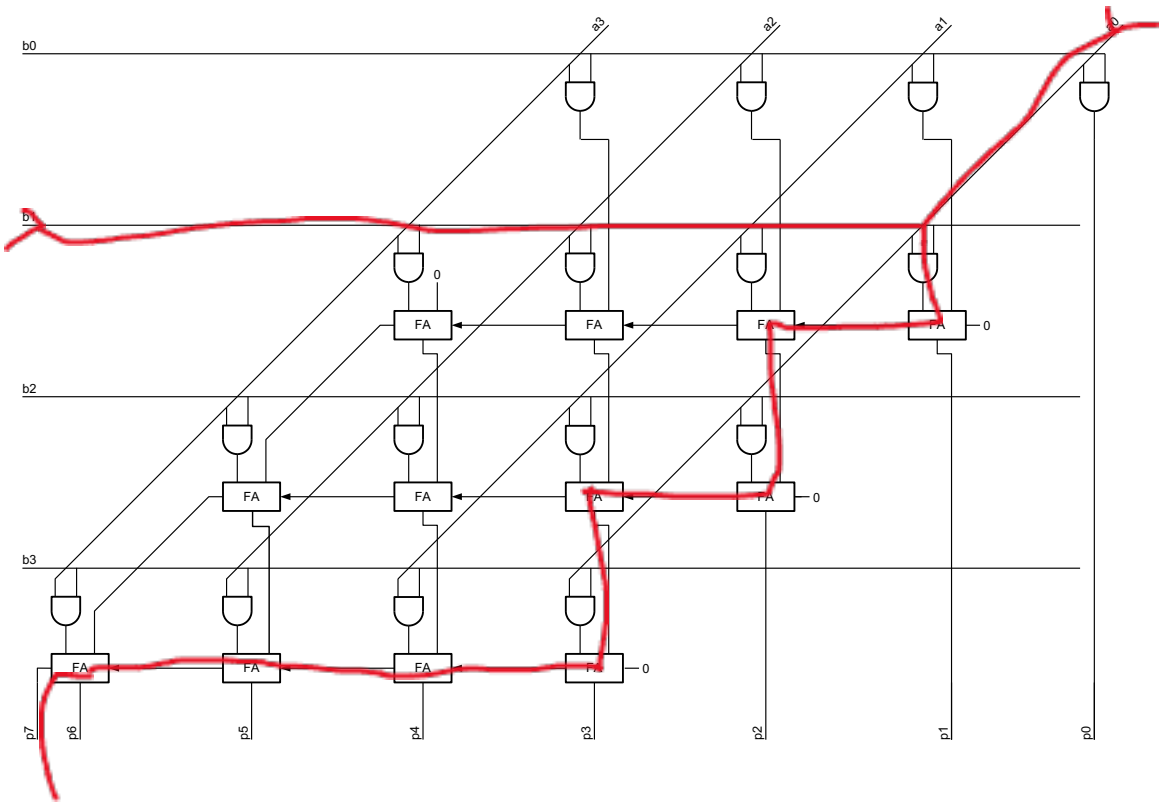
Question 4 Pipeline and Interfaces: (10 points)

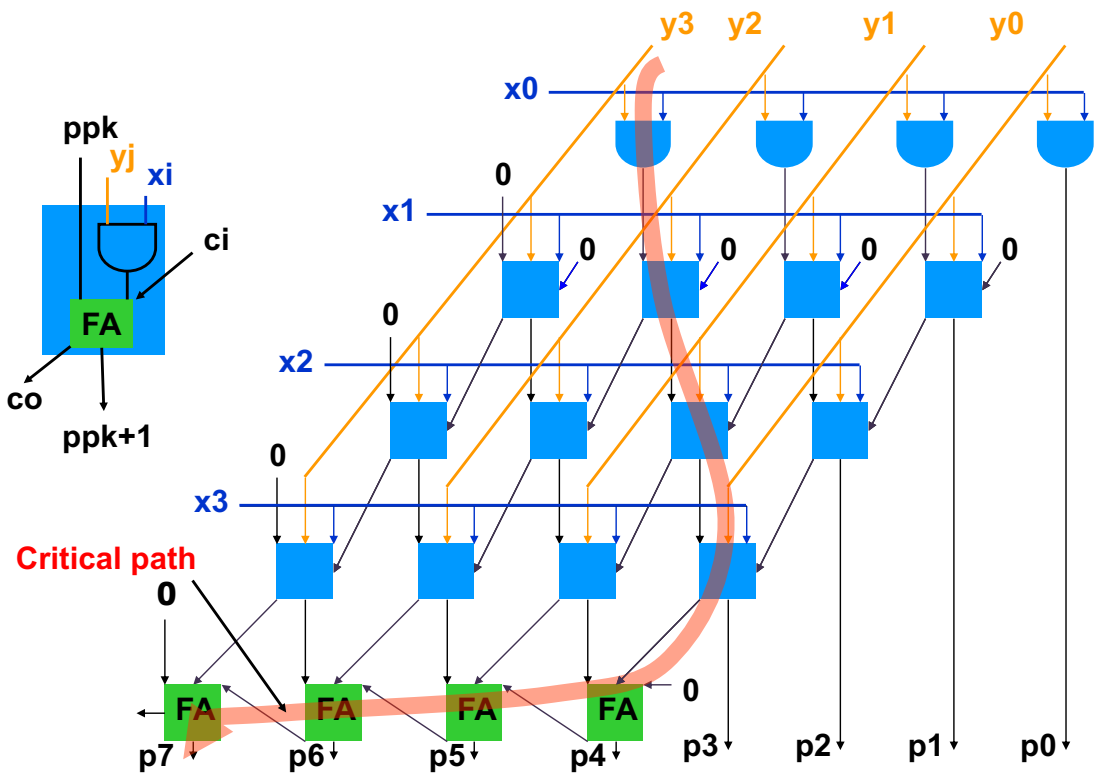
Consider the design of the figure bellow and that:

- a 2-input AND gate has a delay of [a] ns, and
- the delay of a FA (from any of its input to any of its outputs) is [b] ns
- the setup time of a flip flop is [c] ns
- the propagation time of a flip flop is [d] ns

i. Show the critical path of the design and calculate its latency considering that the inputs and the outputs are registered (stored in flip flops).
ii. Calculate the throughput and maximum operating frequency of the design.
iii. pipeline the design in order for the throughput to become [e] times higher. How many pipeline stages are needed?
iv. What is the latency of the pipelined version of the design? What is its maximum operating frequency?

Answer





Above are the critical paths of the circuits used for the variations of the question.

The rest of the question can be answered similar to Exercise 2 in exercise session 7.

i) The critical path includes (1 AND + 8 FA) in the first circuit and (1 AND + 7 FA) in the second circuit as shown in the figures. It starts from an input AND, goes through the first FA to its carry out and continues to other FAs through the carry inputs and outputs until the final carry out is available next to p7. There are FFs on circuit inputs (a and b / x and y) and outputs (p). Therefore, to calculate the critical path latency, we start form the propagation delay from CLK to OUT of the input FF, followed by the logic delay, and finally the setup time of the output FF. This is the minimum time needed between two rising edges of the CLK.
Latency = d + a + 8xb + c (first circuit) or d + a + 7xb +c (second circuit)
For example assuming a =3, b =9, c =1, d =2, e =4 for the first circuit:
L = 78.
If the latency is calculated to be L ns, that is the minimum CLK period, which gives a maximum CLK frequency of 1/L GHz. It also means that we can have 1 set of results per L ns that gives a throughput of 1/L billion operations per second.

ii) To improve the throughput by a factor of e, the latency must be reduced to L/e. So we need to find a way to break the critical path into smaller parts and separate them with FFs, such that the new critical path plus the FF propagation and setup time is smaller than or equal to L/e. With the same

example values, we need to reduce L = 78/4 = 19.5 or smaller. Therefore, we can have a maximum of one FA in each stage because two FAs plus the FF delays becomes 2+18+1 > 19.5. So, in the new pipeline circuit we need to put one FF between each FA in the original critical path. That leads to 8 stages for the 8 FAs in the first circuit.

iii) The critical path in the pipelined circuit is the first stage that also includes an AND gate. So the new critical path latency is 2+3+9+1 = 15 ns. This is the minimum clock period that is equivalent to 66.6MHz maximum frequency or 66.6 M operations per second. But, the new latency is 8x15 = 120ns which is the time it takes to have the final output results, after the data has propagated through the 8 pipeline stages.

Question 5 FSMs: (10 points)
Design a Moore FSM for a vending machine that receives coins of type-1 (1 SEK) and type-2 (2 SEK) and opens when it receives the total amount of 6 SEK. If it receives a larger amount it resets and gives back all the coins it has collected so far.

The FSM should use D flip flops with a reset and a load-enable input.

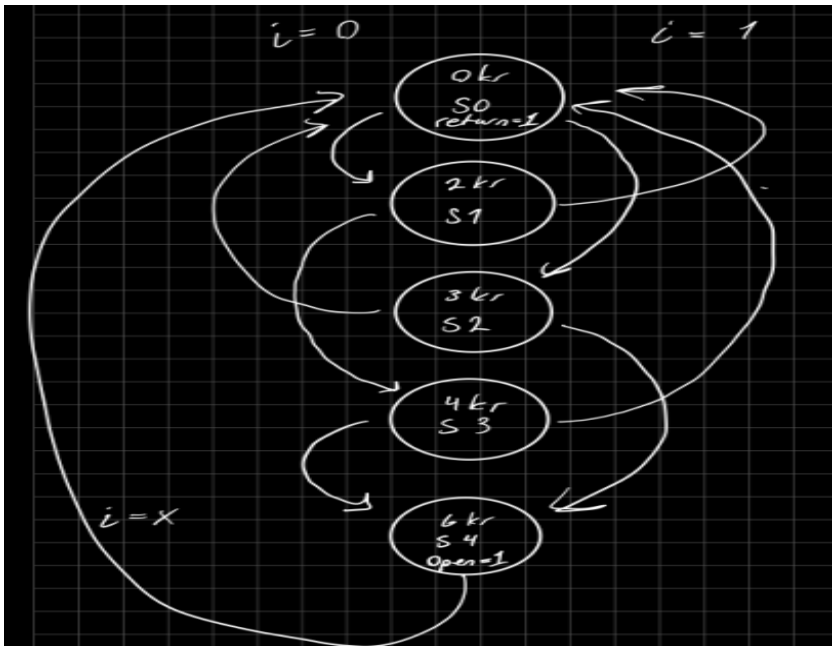
The FSM uses an 1-bit input called coin-type, which is "0" when a type-1 coin is inserted and "1" when a type-2 coin is inserted. When the correct amount is received, the machine reaches its final state, where the output open (Open) is set to “1” in order to accept the received coins and open the product door. After this final state the machine goes back to its initial state. When a larger amount than the expected one is received, then the FSM returns to its initial state. At the initial state a second output (Return) is set to “1”, which returns any received coins.

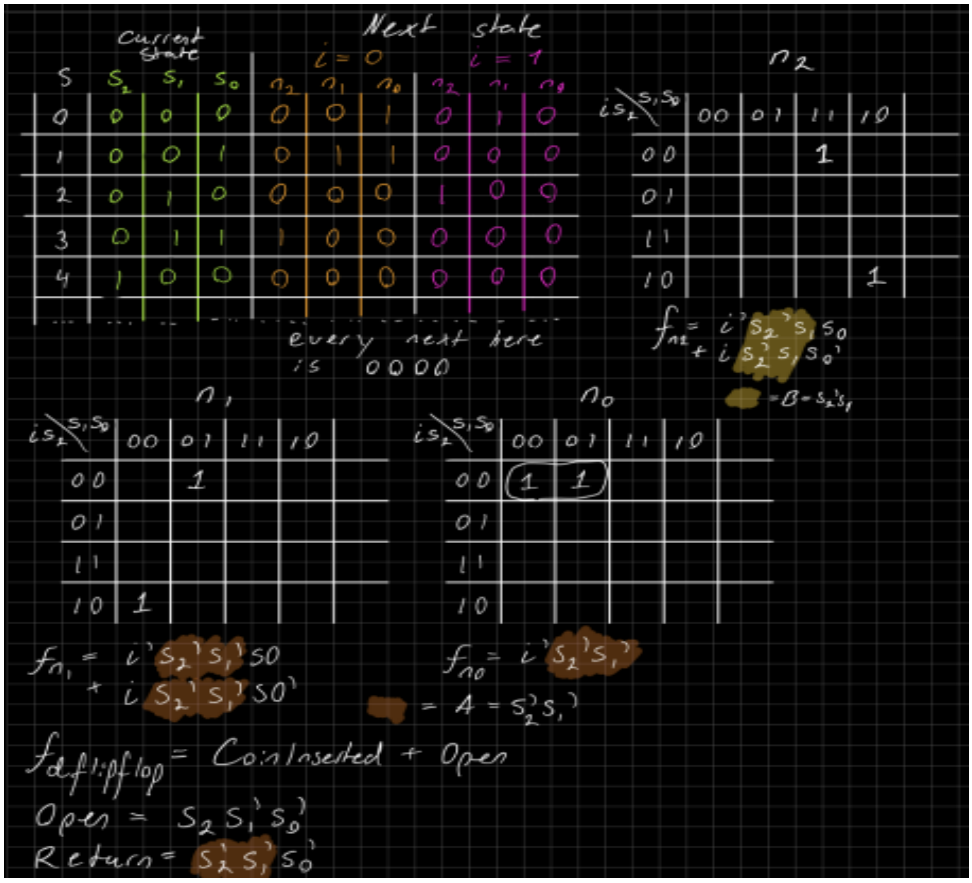
The load-enable of the D flip flops is active when a coin is inserted (input signal coin-inserted = 1) or the FSM output Open is "1".

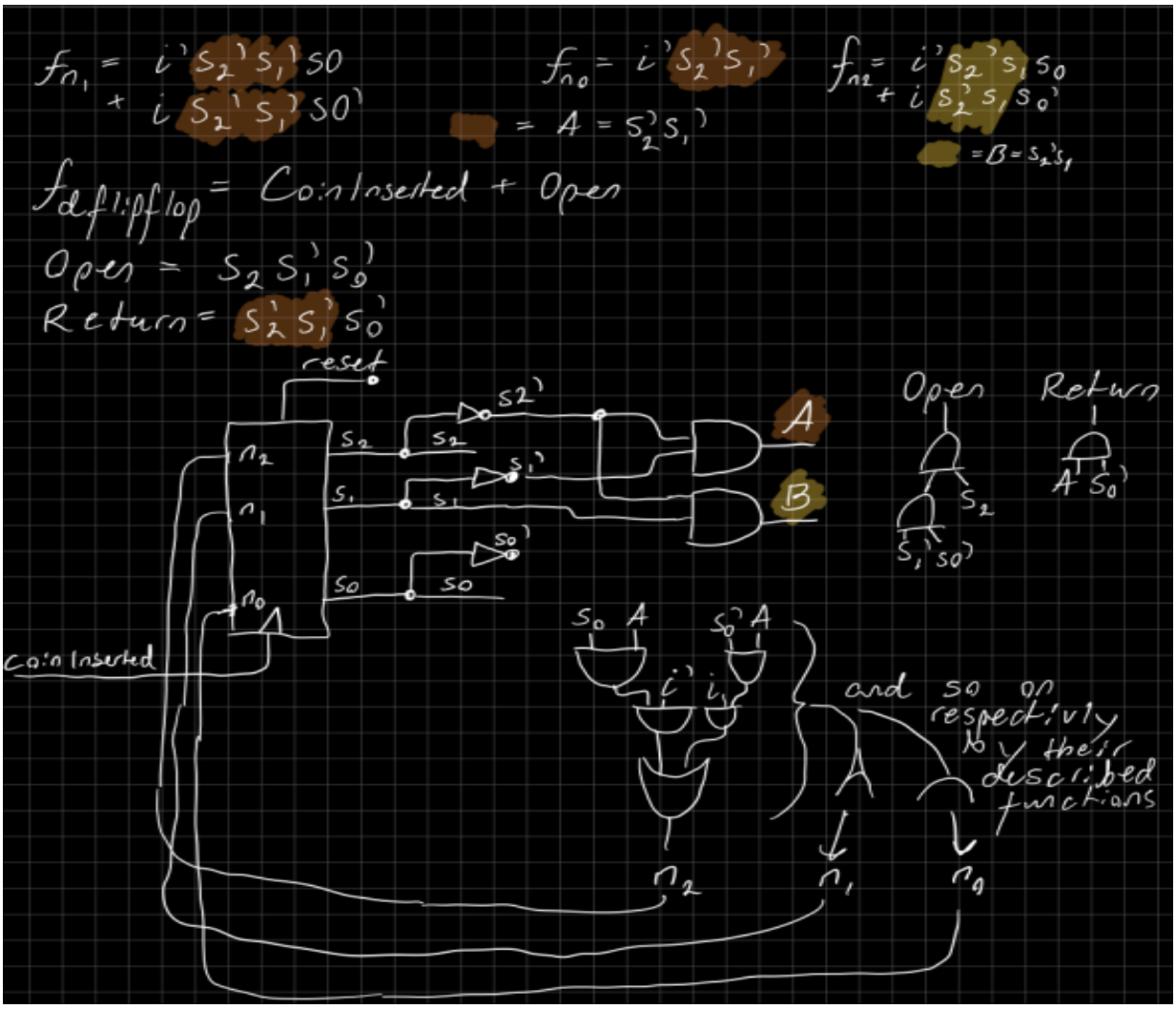
Note that two coins cannot be received at the same time. In addition, when the correct amount is collected, no more coins can be received until the machine resets again.

Make the state diagram and state table, state assignment and implementation of the FSM drawing the gatelevel circuit using D-flip-flops.

Answer
For coins of 2 and 3 SEK and total of 6 SEK.

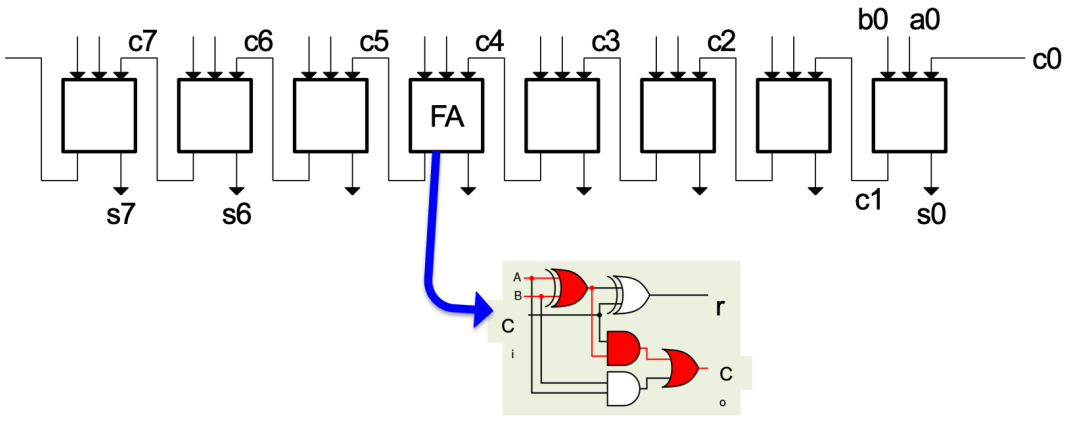

i = 0
i = 1
0kr
S0
return-1
2kr
S1
3kr
S2
4kr
S3
6kr
S4
Open-1
i = x


Current state
Next state
i = 0
i = 1
every next here is 0000
$f_{n2} = i' S_2' S_1 S_0 + i S_2' S_1 S_0' = B = S_2' S_1$
$f_{n1} = i' S_2' S_1' S0 + i S_2' S_1' S0'$
$f_{n0} = i' S_2' S_1' = A = S_2' S_1'$
$f_{d\,flipflop}$ = CoinInserted + Open
Open = $S_2 S_1' S_0'$
Return = $S_2' S_1' S_0'$

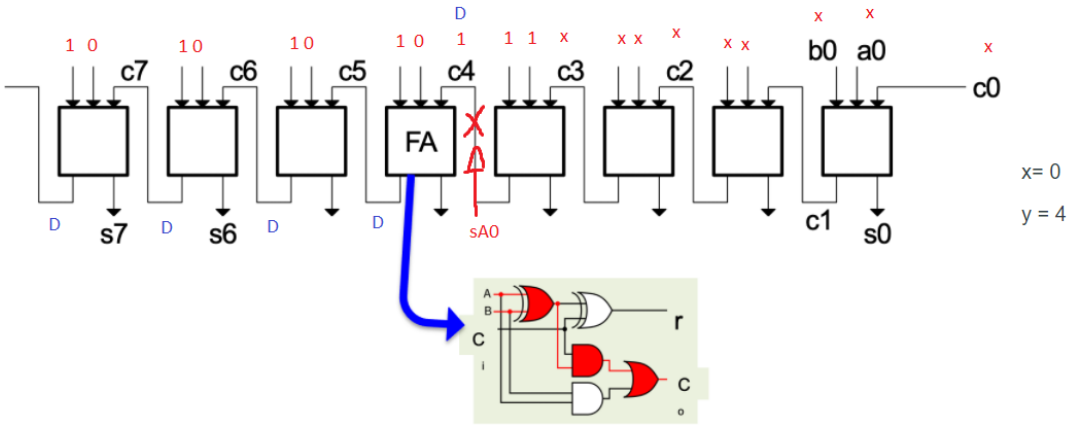


Question 6 Testing: (10 points)

Activate, propagate and justify the stuck-at-[x] fault at the carry-out with index [y] (e.g. if y=1 that is wire c1, if y=2 that is c2, etc.).



Answer
Similar to Lecture on Testing, slides 50-54 and Exercise session 6, Q4.

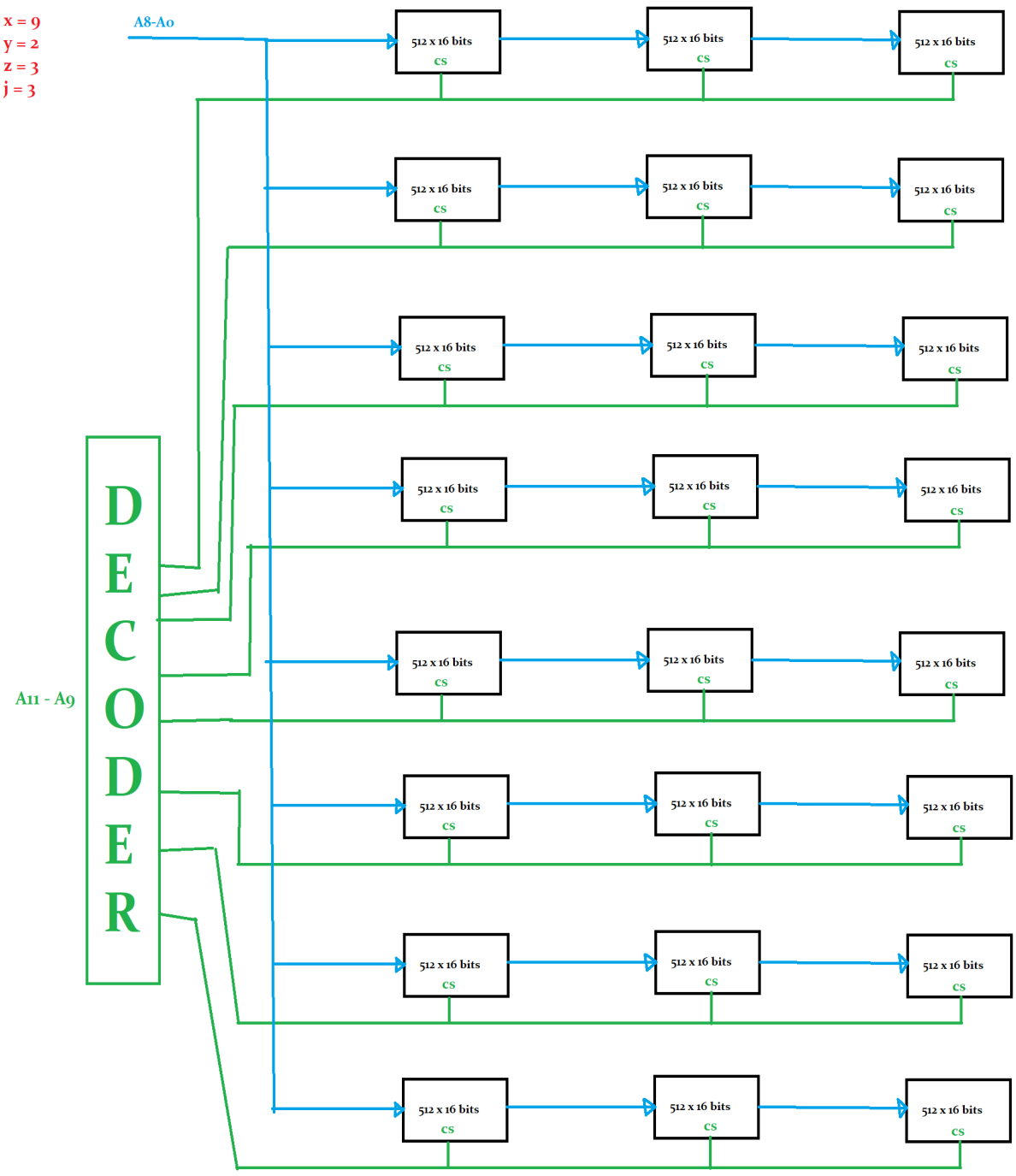


Stuck-at-0 fault at c4.

To activate the fault we need to set c4 to 1, which is the opposite of the stuck value 0. From the generate equation (g = ab) this can be done by setting a3=1 and b3=1. To propagate the fault (D) to the last carry out (c8) we use the propagate equation (p = a ⊕ b) which means a and b need to have different values. So we can set, for example, a4=a5=a6=a7=0 and b4=b5=b6=b7=1. The rest inputs don't care. If c8=0 then there is a stuck-at-0 fault at c4.

Question7 Memory: (10 points)
Use memory blocks that have $2^{[x]}$ entries and each entry has [y]Bytes, to construct a memory of which has $2^{[x+z]}$ entries and [j]*[y] Bytes per entry.
Draw the block diagram of the memory and show how the address bits are connected.

Answer
Similar to Exercise 4 in Exercise Session-6



Question8.1 Asynchronous: (10 points)
Explain the differences between Asynchronous and Synchronous sequential circuits.

Can an Asynchronous sequential circuit be converted to its Synchronous equivalent?

What about the opposite? Can a synchronous sequential circuit be converted to asynchronous? What do you need to pay attention to?

Answer
Synchronous sequential circuits use a clock to control state transitions and flip flops (memory elements in general) to store state. Asynchronous sequential circuits don't use clock and their state variables may change at any point in time. Asynchronous are more vulnerable as hazards and races, but they are probably more power efficient and possibly faster as they don't use flip flops.

An asynchronous sequential circuit can be converted to its synchronous equivalent. In most cases putting flip flops in the feedback loop of the circuit would be sufficient.

The opposite is also possible but it requires attention to races, stability and the fundamental mode restriction which may require to redesign the circuit.

Question8.2 Asynchronous: (10 points)
Explain what is the Fundamental Mode Restriction.
How is it useful?
What will happen if it is violated.

Answer
See Lecture on Asynchronous, slide 5.
It simplifies the analysis of the circuits.
If violated in a circuit that is designed based on this restriction then it may not functioned as expected.

Question8.3 Asynchronous: (10 points)
Explain what is a Critical Race in an asynchronous sequential circuit and how to avoid it.

Answer
See Lecture on Asynchronous, slide 21-24.

Question8.4 Asynchronous: (10 points)
Explain what is the stability in an asynchronous sequential circuit.
Why is it important?
Explain what happens if an asynchronous circuit is unstable for a particular input combination.

Answer
See Lecture on Asynchronous, slide 5.
It is important because the circuit can function in a controlled way only when it is in stable states.
If for an input combination there is no stable state then the circuit will be in a cycle, indefinitely looping between unstable states until the input values change (examples in slides 32, 37).

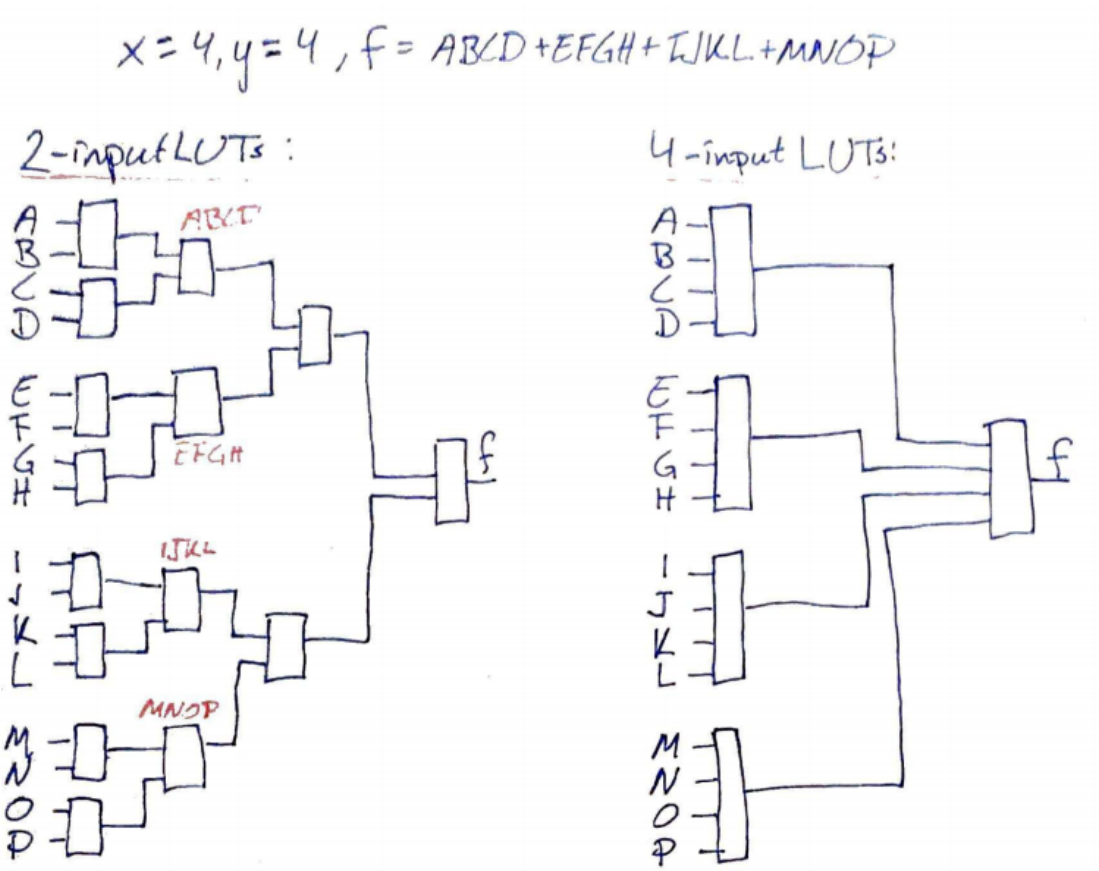
Question 9 Reconfigurable Technologies: (10 points)
Consider a Boolean function that is a sum of [x] products with each product of the function having [y] unique inputs. Map the function in the SRAM-based Lookup Tables (LUTs) of the following two FPGA devices. The first FPGA has 2-input LUTs and the second FPGA has 4-input LUTs.

- How many LUTs are used in each FPGA device?
- How many SRAM bits in total are used in each FPGA device?
- Which FPGA device will use more wire resources?

Answer
Similar to lecture on reconfigurable hardware, slide 19

Assume x=4, y=4: f = ABCD + EFGH + IJKL + MNOP

- For 2-input LUTs we need 3 LUTS to create one product. These then need to be connected, resulting in 15 LUTs in total. For 4-input LUTs we need 1 LUT per product, and then 1 LUT to connect them, resulting in 5 LUTs in total.
- The number of SRAM bits is 4 per 2-input LUT and 16 per 4-input LUT, giving us a total of: 4*15 = 60 SRAM bits for the 2-input version and 16*5 = 80 SRAM bits for the 4-input version.
- The version with 2-input LUTs will require more interconnects between them and therefore use more wire resources (count the number of lines between the LUTS in the picture).



Question 10 Delay and Power: (10 points)
Consider that all inputs and outputs of the following 2 combinational circuits are registered (stored in D-flip flops) and that:

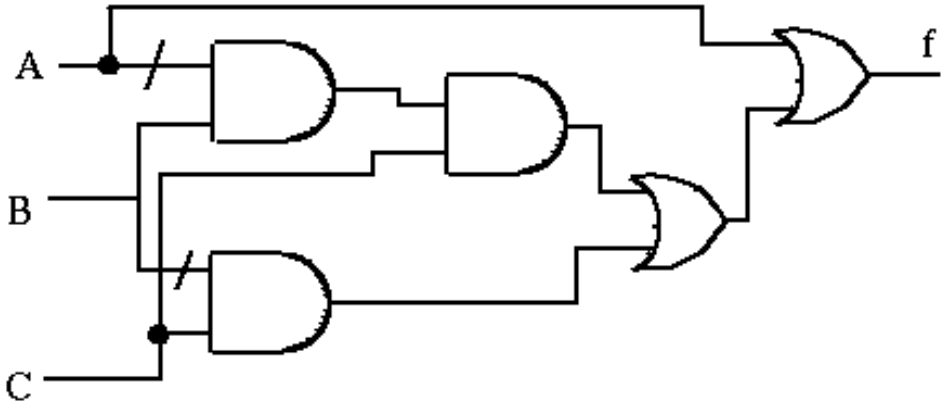
a 2-input AND/OR gate has a delay of [x] ns,
a 2-input XOR gate has a delay of 2*[x] ns,
the setup time of a flipflop is [y] ns, and
the propagation time of a flip flop is [z] ns

Compare the dynamic power of the two circuits when:

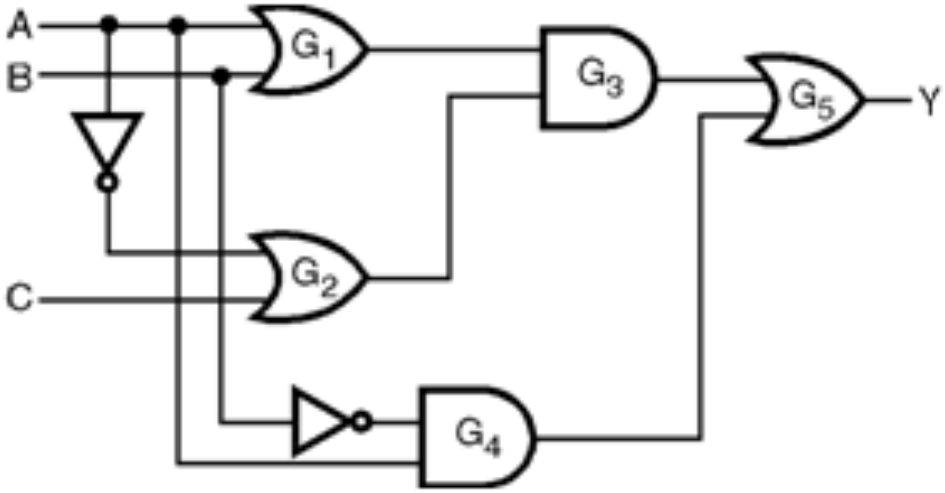
- both circuits operating at their maximum frequencies
- both circuits have the same voltage, capacitance, and input activity
- a D-flipflop has the same dynamic power with a 2-input AND/OR gate
    - a D flip flop as well as a 2-input AND/OR gate count as one node each in the circuit
- a 2-input XOR gate has the same dynamic power with a 2-input AND/OR gate.
    - a 2-input XOR gate as well as a 2-input AND/OR gate count as one node each in the circuit

Note that inverters are considered to have zero delay and zero dynamic power.

Version 1:

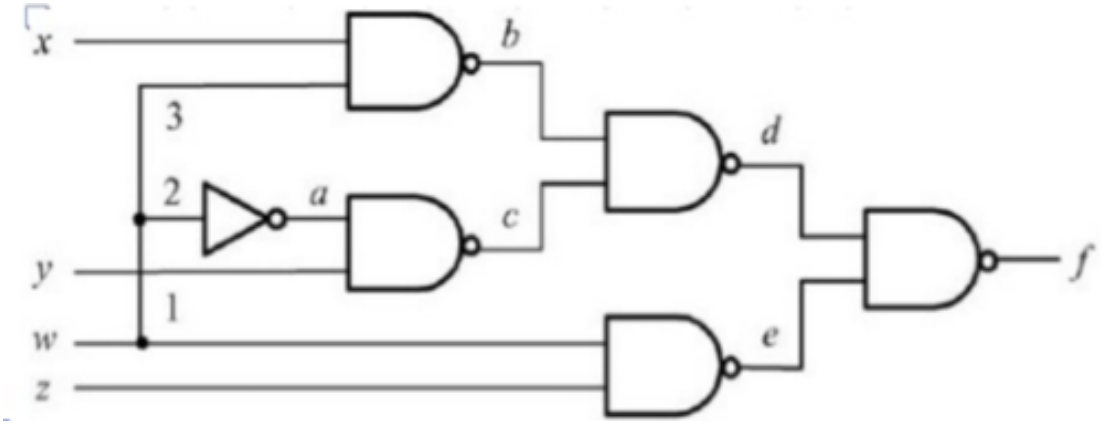


(combinational circuit 1)

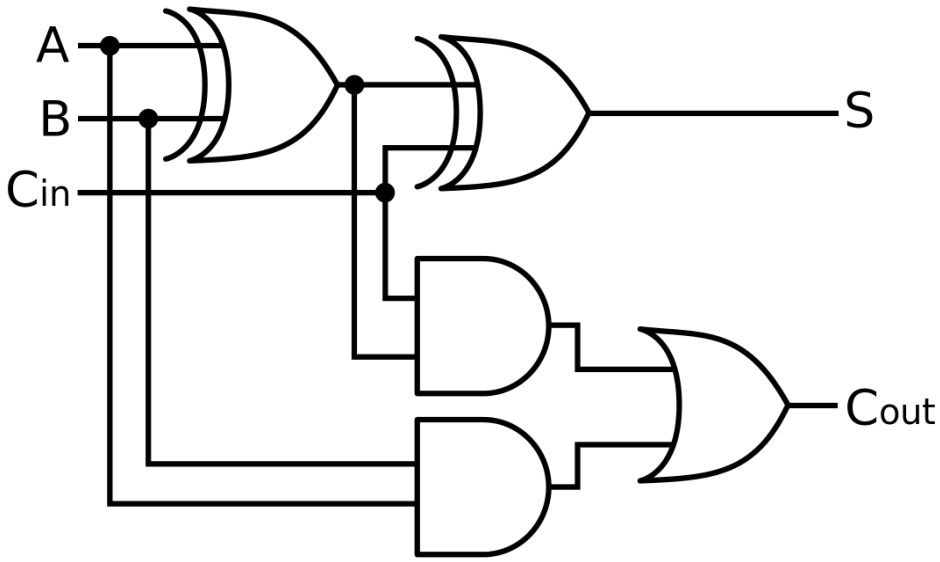


(combinational circuit 2)

Version 2:



(combinational circuit 1)



(combinational circuit 2)

Answer:

find the critical path delay of the circuits, the inverse gives the frequency **f**.
Count the number of gates and flip flops in each design, **n**.

Calculate the dynamic power using the following equation (all other parameters are equal for the two circuits)

$$P_{avg} = n \cdot \alpha_{avg} \cdot f \cdot c_{avg} V_{dd}^{\ 2}$$

For example assuming x = 10, y=z=1 for Version 2:

Critical Path 1 : Input FF + 3 NAND + 1 NOT + Output FF : L = 1+3x10+1 = 32 ns -> f = 32.25 MHz
Critical Path 2 : Input FF + (2 XOR or AND+OR) + Output FF = 1+2*20+ 1 = 42ns -> f = 23.81 MHz
The gate count is the same. So the only parameter that affects power is frequnecy.
P1/P2 = f1/f2 = 32.25/23.81 = 1.35
That meas circuit 1 has 35% more power because of its higher frequency.

END of EXAM