EDA322/ DIT797: Digital Design
Exam - March 2020

Date: March 18, 2019

Time: **14:00-18:00**

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Department: Computer Science and Engineering

Inquiries: contact through phone, phone extension 1744

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: a calculator, lecture notes, textbook, etc. are allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Question 1 Arithmetic: (10 points)
Show the contents of the registers in a serial 4-bit multipler/divider that performed it performs the operation [x]/[y]
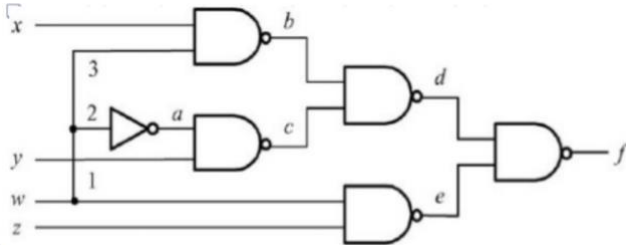
Answer
Lecture on Arithmetic slide 11 for multiplication and slide 25 for divider.

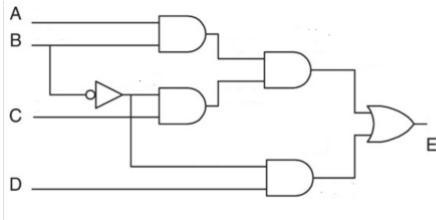**Question 2** Hazards: (10 points)
a) Show a dynamic hazard in the following circuit. Consider the NAND gates and the inverter
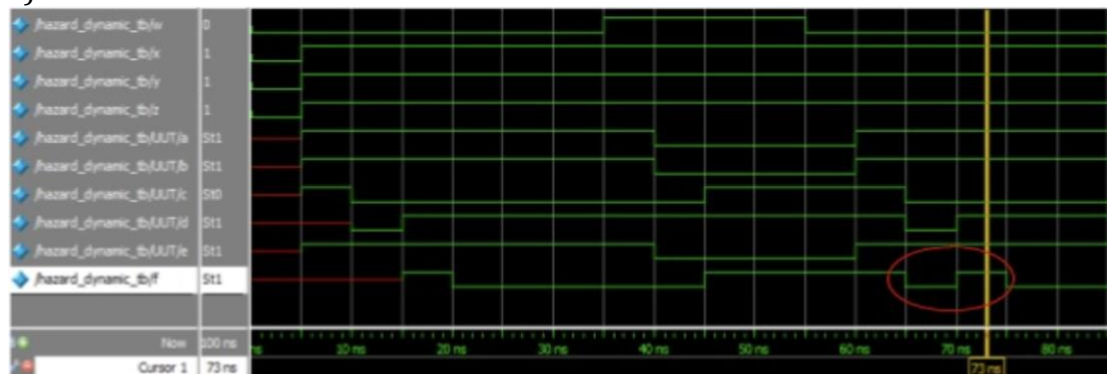
circuit-1:

Or
circuit-2
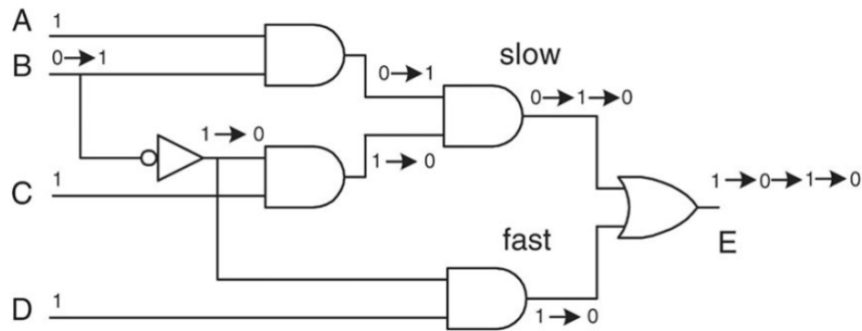

b) Draw a hazard-free equivalent of the circuit.

Answer
a) circuit-1

Or
circuit-2

b) Make the truth table of the function, make it's K-map, regenerate the function.
circuit-1

w	x	y	z	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

$F = F = x'w + w'y' + wz + x'y' + y'z$

circuit-2: is solved similar to circuit-1

Question 3 Number representation: (10 points)
Suppose you need to represent distance from 1 centimeter (cm) to 10 meters (m) with an accuracy of 5%.
   a) Find a fixed point representation that fits the above specification
   b) Find a floating point representation that fits the above specification
   c) Which type of the above number representations is better and why?

Answer
   a) 5% of a cm accuracy is 0.5 millimeters (mm).
      This needs a resolution of 2*0.5 mm = 1 mm = 1/1000 meters.

If meters is the integer part we need, then we need 4 bits for integer (to count between 0-10 meters). Then, the fraction needs 10 bits to count $1/2_{10} = 1/1024$ meters (which is a bit shorter than 1 mm resolution). So the fixed-point representation would require 14 bits (4.10).
Alternatively, we can count millimeters which is the required resolution. 10 meters = 10000 mm for which we need again 14 bits (2_{14}=16K).

b) For a floating-point representation, the mantissa needs to be only 4 bits to offer accuracy of 5%. So, the resolution needs be double that: 10% = 1/10; $1/16= 1/2^4$ should then be enough (4 bits mantissa). The dynamic range is from 1cm (10_{-2}m) to 10_1 m so it is 10^3, which is smaller than 1024 = 2^{10}. Then, 4 bits are enough to count up to 10, so with 4-bits exponent we can represent a range of 2^{16} (which is larger than 2^{10}). We finally set the bias to 12 so the maximum exponent to be 2^{16-12} = 2^4 =16 >10, since the largest number to represent is 10 meters. So, the floating point format is 4 bits mantissa and 4 bits exponent.

c) Floating point needs fewer bits than fixed point, so it is a better choice. That happens because the required accuracy is a percentage and not a fixed absolute value.

Question 4 Pipeline and Interfaces: (10 points)
   a) Consider an unpipelined 16-bit Ripple Carry Adder. Consider also that the delay of a Full Adder is 100 ps, the setup time of a flipflop is 120ps and the propagation time is 75ps. What is the larger number of stages we can pipeline the ripple carry adder before its latency gets double the latency of the unpipelined version?
   b) Show the interfaces between two pipeline stages A and B. Show their timing diagram considering that stage A has a delay of 2 cycles and stage B has a delay of 5 cycles. The timing diagram needs to start on the cycle that A starts producing a result for a problem X and should end when B completes the processing of the same problem X.
   c) What would you do to balance the pipeline?

Answer
a) latency of unpipelined RCA: 16*100= 1.6 ns
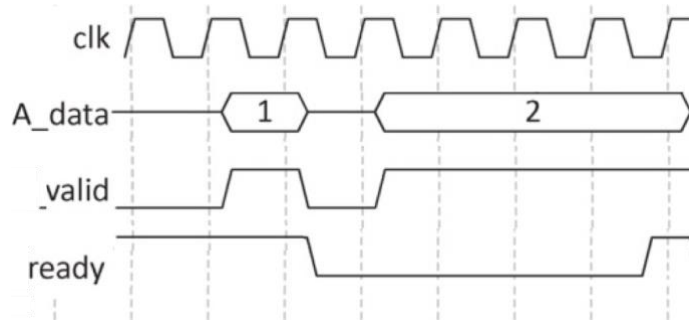with 8 stages the additional latency is 8*(120+75) = 1.56ns
with 9 stages the additional delay would be 1.755ns.
So 8 stages is the answer, each stage adding 2 bits (out of the 16 bits), so each stage would need 2 FAs.

The throughput of the 8-stage pipelined design would be one result every 200+195 ps = 395ps which is 2.532 Giga ops per second.
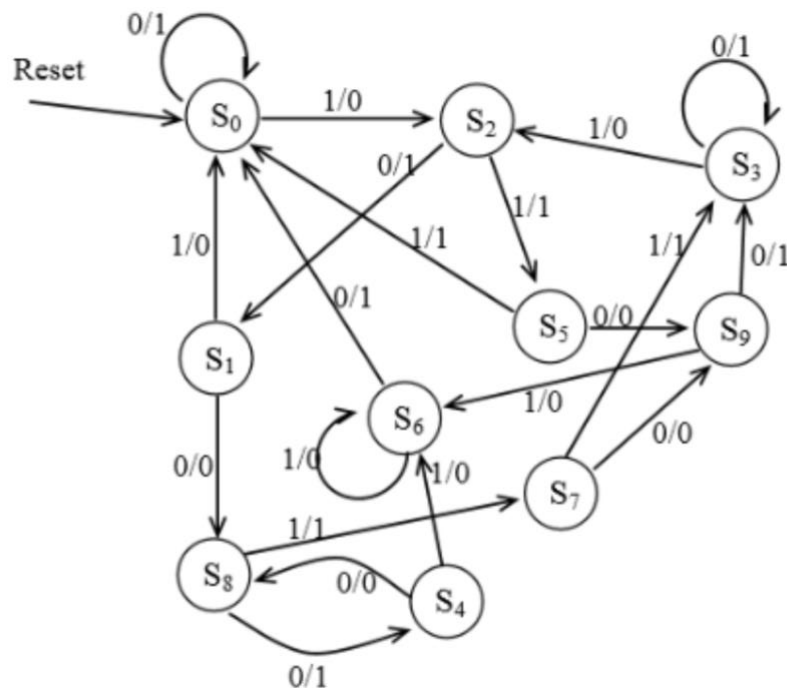b)

c) Since this is a static and not variable unbalance, a way to balance the pipeline would be to split B in multiple stages or replicate it.
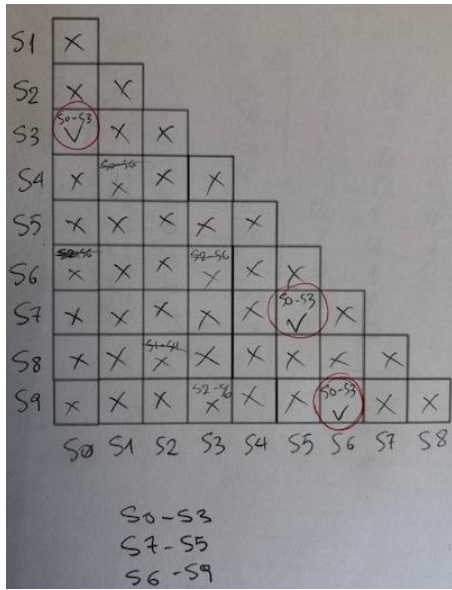
Question 5 FSMs: (10 points)
The state diagram defines an FSM with an Input X and an output Z.
a) Minimize the number of states of this FSM and list the equivalent states.
b) Draw the state diagram and state table of the reduced FSM.
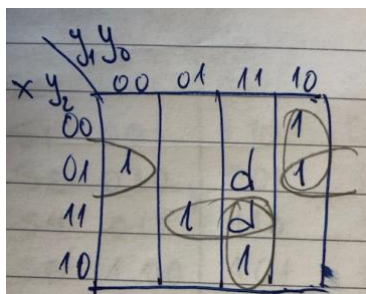c) derive the Boolean functions for the next state bits and the output of the reduced FSM.
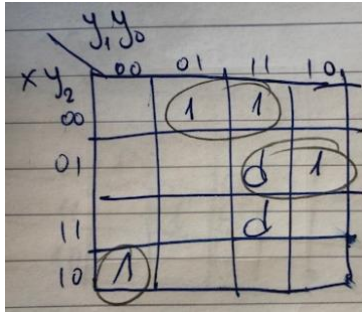

Answer

Implication chart (rows S1–S9, columns S0–S8):

	S0	S1	S2	S3	S4	S5	S6	S7	S8
S1	×								
S2	×	×							
S3	✓ (S0-S3)	×	×						
S4	×	× (S0-S5)	×	×					
S5	×	×	×	×	×				
S6	× (S2-S6)	×	×	× (S3-S6)	×	×			
S7	×	×	×	×	×	✓ (S0-S3)	×		
S8	×	×	× (S1-S4)	×	×	×	×	×	
S9	×	×	×	× (S2-S6)	×	×	✓ (S0-S3)	×	×

S0 - S3
S7 - S5
S6 - S9

Pres.	Next State X=0	X=1	Output X=0	X=1
S0	S0	S2	1	0
S1	S8	S0	0	0
S2	S1	S5	1	1
S3	S3	S2	1	0
S4	S8	S6	0	0
S5	S9	S0	0	1
S6	S0	S6	1	0
S7	S9	S3	0	1
S8	S4	S7	1	1
S9	S3	S6	1	0

Pres State	Next State X=0	X=1	Output X=0	X=1
S0'	S0'	S2	1	0
S1	S8	S0'	0	0
S2	S1	S5'	1	1
S4	S8	S6'	0	0
S5'	S6'	S0'	0	1
S6'	S0'	S6'	1	0
S8	S4	S5'	1	1

Pres. State	$y_2 y_1 y_0$	Next State X=0 $Y_2 Y_1 Y_0$	X=1 $Y_2 Y_1 Y_0$	Output (z) X=0	X=1
S0	000	000	010	1	0
S1	001	110	000	0	0
S2	010	001	100	1	1
S4	011	110	101	0	0
S5'	100	101	000	0	1
S6'	101	000	101	1	0
S8	110	011	100	1	1
	111	d	d	d	d

Karnaugh map for Y_0 (rows xy_2: 00, 01, 11, 10; columns $y_1 y_0$: 00, 01, 11, 10):

$xy_2 \backslash y_1y_0$	00	01	11	10
00				1
01	1		d	1
11		1	d	
10			1	

$Y_0 = x'y_1 y_0' + x'y_2 y_0' + x y_2 y_0 + x y_1 y_0$

$Y1 = x\,y_2'\,y_1'\,y_0' + x'\,y_2'\,y_0 + x'\,y_2\,y_1$
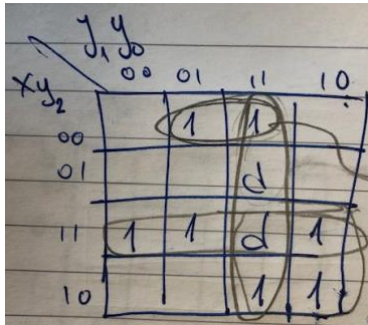
$Y2 = x'\,y_2'\,y_0 + y_1\,y_0 + x\,y_2 + x\,y_1$
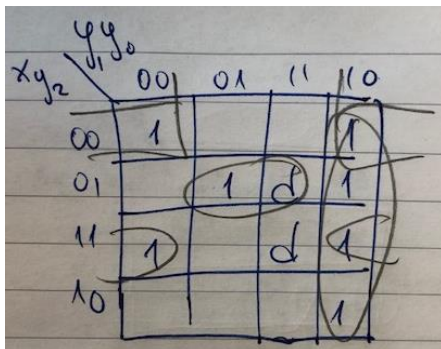
$Z = y_1\,y_0' + x'\,y_2'\,y_0' + x'\,y_2\,y_0 + x\,y_2\,y_0'$

Question 6 Testing: (10 points)
Activate, propagate and justify the stuck-at-[x] fault at the output of gate [y].
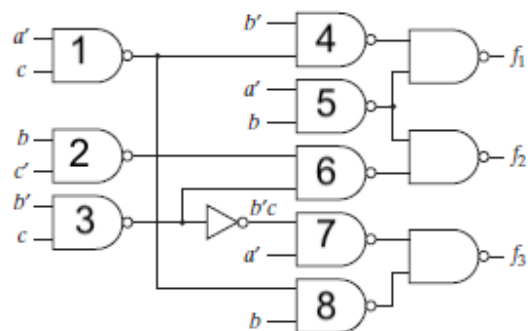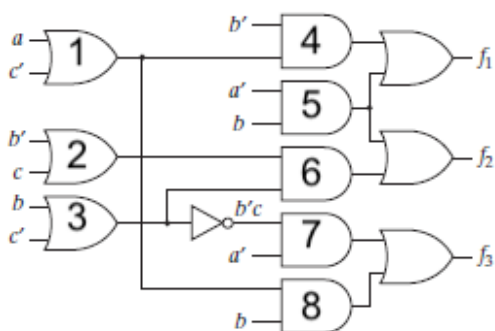
Answer

Similar to Lecture on Testing, slides 50-54

Question7 Memory: (10 points)
Use memory blocks that have $2_{[x]}$ entries and each entry has [y]Bytes, to construct a memory of which has $2_{[x+z]}$ entries and [j]*[y] Bytes.
Draw the block diagram of the memory and show how the address bits are connected.

Answer
Similar to Lecture on memory, slide 23

Question8 Sequential circuits: (10 points)
   a) Describe what is the setup time, hold time and propagation time of a flip flop.
   b) Consider that setup time = [x] ns, hold time = [y] ns, and propagation time =[z] ns. Explain if two cascaded flip-flops (one giving input to the other) with these timing characteristics would operate correctly, and why.
   c) If they would operate correctly what would be their maximum operating frequency? Otherwise, if they would not operate correctly, explain what can happen in the second flip flop and why.
   d) Consider now that hold time = [z] ns, and propagation time =[y] ns and answer (c) again.

Answer
a) Lecture on Timing Delay and power, slide 19 (also lecture on Sequential circuits slide 21)
b+c+d) check condition Tp>Th as explained in Lecture on Timing Delay and power, slide 21

If the above condition is met then clock period >Ts+Tp

If the condition is not met the second flip flop will get in a metastable state

**Question 9** Reconfigurable Technologies: (10 points)
Draw the block diagram of a 4-input programmable gate in an FPGA. Show its configuration when its programmed to implement a 4-input logic **NAND** gate.

Answer
Lecture on Reconfigurable Hardware, slide 15, and similar to slide 18 (make truth table of NAND and load it to the 16bits of the LUT).

Question 10 Arithmetic & Timing: (10 points)
a) Show the critical path of the 4-bit array multiplier of the figure below.
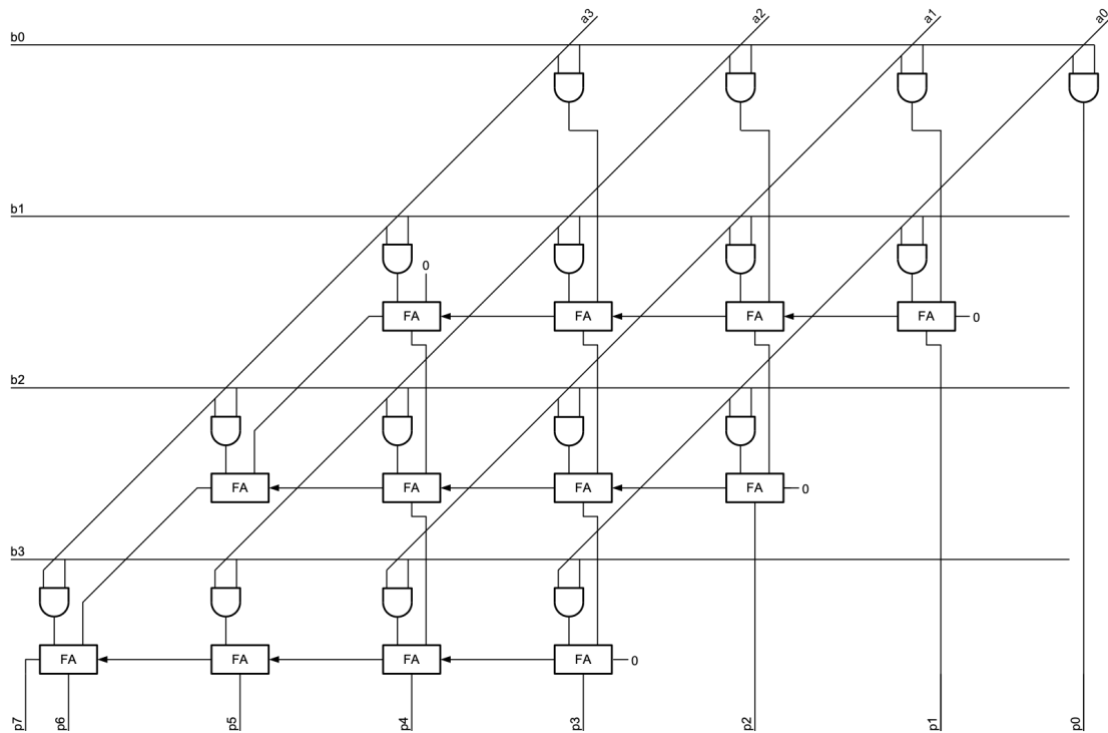
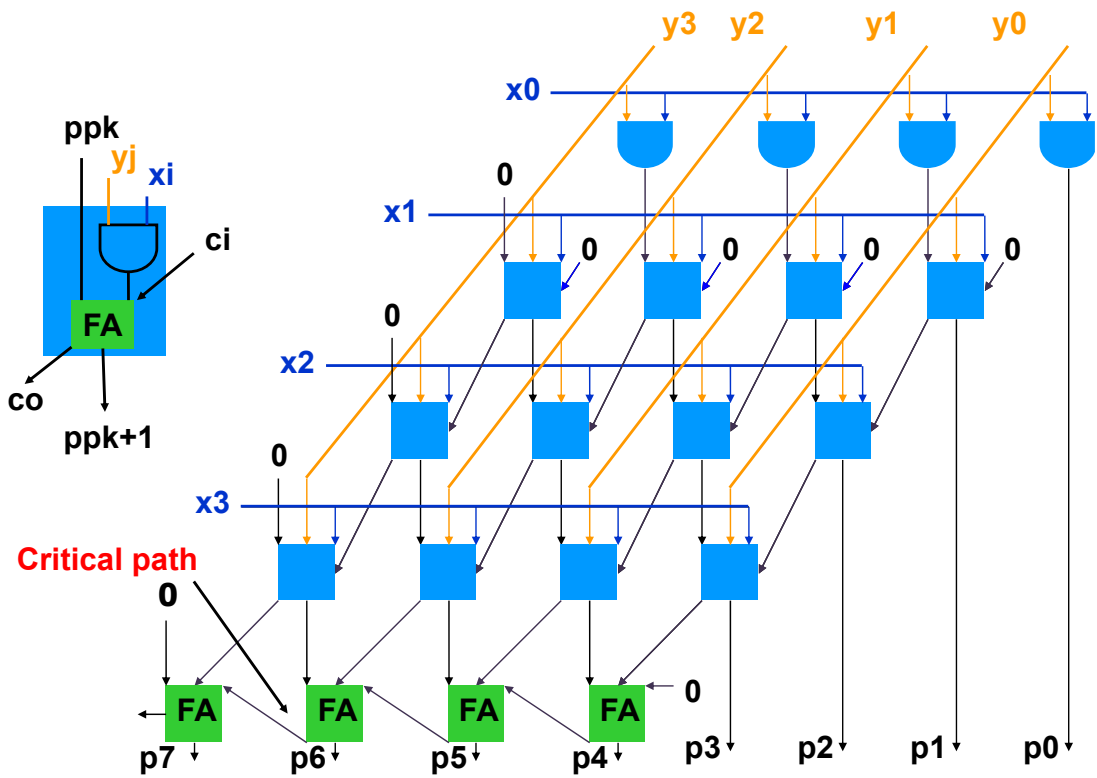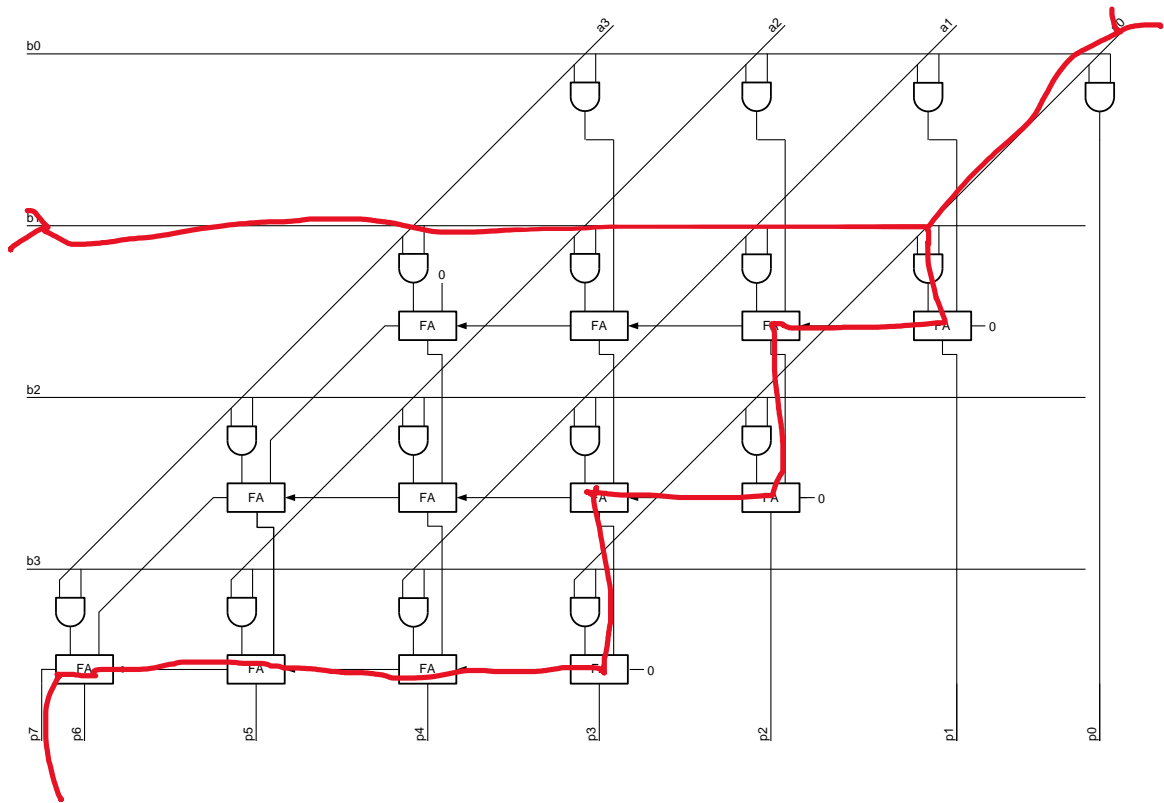Describe from which inputs it starts, through which gates/modules it goes through, and were it ends.

Consider that a 2-input XOR gate has a delay of [x] ns and a 2-input AND/OR gate have a delay of [y] ns. What is the delay of the critical path?

You can also consider the following full adder circuit:
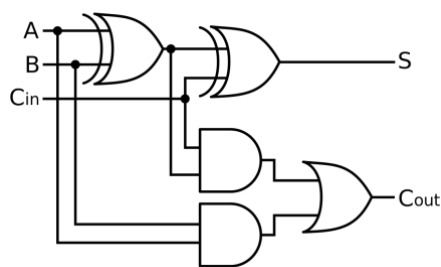
b) Change the design of that 4-bit array multiplier to reduce its critical path. What is the delay of the critical path now?

Answer:

END of EXAM