EDA322/ DIT797: Digital Design
Exam - June 2019

Date: June 12, 2019

Time: **14:00-18:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries: visiting the room at **15:30** and at
17:00
(contact through phone: phone extension 1744)

Results and grading review: room 4128 EDIT on **June 28th at 11:00**.

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: a calculator is allowed. No textbooks or lecture notes, etc. allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

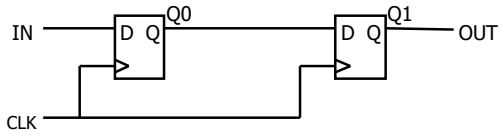
Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Question 1 Sequential Circuits & Timing: (10 points)
Explain the timing characteristics of a flip-flop and show how they need to relate with each other in order for two (or more) cascaded flip flops to function correctly as a shift register (shown in the figure below).



Question 2 Arithmetic & Timing: (10 points)
Draw the gatelevel block diagram of a 4-bit array multiplier, find its critical path and measure its delay considering that a:

- 2-input AND gate has a delay of 1ns
- 2-input OR gate has a delay of 1ns
- 2-input XOR gate has a delay of 2ns

Question 3 Interfaces: (10 points)
Consider a FIFO (first-in-first-out) (also known as Queue) were words can be enqueued as long as the FIFO is not full and words can be dequeued as long as the FIFO is not empty. Describe the FIFO interfaces for enqueuing words and for dequeuing words.

Question 4 Pipelining: (10 points)
Consider that a pipeline is composed of the two stages bellow: *Xform* with latency L and *Clip* with latency 2*L.

- What is the throughput of the pipeline?
- What are the two methods to improve the throughput of the pipeline and achieve load balancing?
- What is the throughput then?

Question 5 FSM (10 points)
Design a Moore FSM that detects a sequence of 3 or more consecutive 1's in a 1-bit input "IN". Consider D-flip-flops for the FSM implementation with clock "CLOCK" and synchronous reset "RESET".

Question 6 Testing: (10 points)
Consider that for a specific technology the produced chips with area *A* have a yield Y=0.6, defect density d=1 and clustering parameter α=1. How should *A* change in order for the yield to become Y'=0.9?

Question 7 Hazards: (10 points)
Show and eliminate the hazards in the following Boolean function:

$$F = (A + C)(A' + D')(B' + C' + D)$$

Question 8 Memory: (10 points)
Describe the sequence of commands sent to DRAM for reading one DRAM word.

Question 9 Arithmetic: (10 points)
Compare the design of a (i) ripple carry adder, (ii) carry-select adder, and (ii) carry lookahead adder in terms of a) area, and b) delay, with respect to the number of operant bits.
Note: use big O notation to show how area and delay change with respect to the number of operand bits (N).

Question 10 Reconfigurable Technologies: (10 points)
Describe the hardware block used in FPGA devices to implement a programmable gate. Show an example of a 3-input Boolean function mapped to such a programable gate.

END of EXAM