EDA322/ DIT797: Digital Design
Exam - June 2018

Date: June 8, 2018

Time: **14:00-18:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries: Ioannis Sourdis (extension 1744); will visit the room at **15:30** and at **17:00**

Results and grading review: room 4128 EDIT on **June 29th at 11:00**.

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%

GU:
Fail(U): 0%-49%, Pass(G): 50%-79%, Pass with Distinction(VG): 80%-100%

Available references:
a calculator is allowed. No textbooks or lecture notes, etc. allowed.

General:

Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Question 1 Sequential Circuits: (10 points)
Draw the (i) gatelevel block diagram, (ii) the truth table and (iii) the state-diagram of a NAND-based SR-latch.

Question 2 Interfaces: (10 points)
Give one example of a digital module that uses each of the following interfaces:

(i) a flow control interface,
(ii) a push flow control interface, and
(iii) a pull flow control interface.

Explain your choices.

Question 3 FSMs: (10 points)
Minimize the states of the FSM described by the following state table.

Current State	Next State		Output	
	Input X		*Input X*	
	0	1	0	1
0	7	2	0	0
1	7	5	0	0
2	7	0	1	0
3	0	7	1	0
4	3	6	0	0
5	3	1	1	0
6	3	4	1	0
7	4	3	1	0

Question 4 Asynchronous: (10 points)
a) Detect any race conditions in the asynchronous circuit defined by the following state table:

State	Code (c,a,b)	Next (in) 0	Next (in) 1	Out (a,b)
A	000	(A)	B	00
B	110	C	(B)	10
C	100	(C)	D	00
D	001	A	(D)	01

b) Make the necessary modifications to eliminate race conditions

Question 5 Pipelining: (10 points)
Consider that an instruction requires to go through (all) the following microprocessor steps in order to be executed:

1. **Fetch**: instruction read
2. **Read:** registers (operands) read
3. **ALU:** execute instruction
4. **Mem:** Data memory access
5. **Write:** write back result to registers

Consider the following delays:

- Fetch 1 ns,
- Read 0,8 ns,
- ALU 1,1 ns,
- Mem 1 ns,
- Write 0,8 ns
- Setup time of a flipflop 0,1ns
- Propagation time of a flipflop 0.1ns
- Hold time of a flipflop 0,05ns

What would be the latency and throughput of the microprocessor if
a) the above steps are performed in one cycle (unpipelined).
b) the microprocessor is pipelined and each of the above 5 steps is a separate pipeline stage.

Question 6 Testing & Timing: (10 points)
Draw the gate-level block diagram of a 4-bit ripple carry adder.

a) How would you modify the adder to also support subtraction?
b) Find the critical path delay of the circuit in (a) if a 2-input XOR gate has a latency of 2 ns and a 2-input OR or AND gate has a latency of 1 ns.
c) Find two input test vectors for the circuit in (a), one testing for a stuck-at-1 and the other for a stuck-at-0 in the carry-in signal of the 4^{th} full adder.

Question 7 Timing: (10 points)

a) What is clock skew and how can it be avoided?
b) What is metastability and how can it be avoided in a flip flop with asynchronous input?

Question 8 Memories: (10 points)
a) Draw the gatelevel block diagram of a 4x3 memory block (4 entries of 3 bits wide) without showing the internals of a single bit memory cell.
b) Create a 8x6 memory made out of the above 4x3 memory blocks. Draw the new gatelevel block diagram (no need to draw again the internals of the 4x3 block). What is(are) the name(s) of the mechanism(s) used to create the new memory?

Question 9 Arithmetic: (10 points)
Draw the block diagram and describe the functionality of a 3-bit sequential divider. Show how you can use it to perform the division 7/3.

Question 10 Reconfigurable Hardware: (10 points)
Consider the implementation of the following function:

$$F = A_0A_1A_3 + A_1A_2\bar{A}_3 + \bar{A}_0\bar{A}_1\bar{A}_2$$

in 3 different FPGAs, each composed of logic cells with either (i) 4-input LUTs, (ii) 3-input LUTs, or (iii) 2-input LUTs.

a) Show the mapping of the logic of function F in each of the 3 types of FPGAs. How many LUTs are needed in each case? How many bits of SRAM memory needed in total for each case?

b) Which is the most efficient choice of LUT size in terms of area? What happens to the delay of the function implementation in each case?

END of EXAM