EDA321/EDA322: Digital Design
Exam - March 2016

Date: March 16, 2015

Time: **14:00-18:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries: Ioannis Sourdis (extension 1744); will visit the room at **15:30** and at **17:00**

Results and grading review: See me in my office 4110 on **April 12th at 10:00**.

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: Blank paper and a calculator are allowed. No textbooks or lecture notes, etc. allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Question 1: (10 points)
Minimize the cost of function F (x3,x2,x1,x0)= Σ(3,4,8,11)+D(0,1,7,9,15) using Quine-McCluskey (x0 is the list significant bit, x3 is the most significant bit).

Measure the cost of the minimized function by counting the total number of 2-input gates of the circuit (inversions are not considered) e.g., a*b + c*d, has cost of 3.

Answer:

Truth table for the minterms Σ(3,4,8,11):

i	x3	x2	x1	x0	y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

Truth table for the don't care terms D(0,1,7,9,15):

i	x3	x2	x1	x0	h*
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	1

The minterms and don't care terms are put together:

Step 1:

Indexgruppe	Index
0	0 *
1	1 * 4 * 8 *
2	3 * 9 *
3	7 * 11 *
4	15 *

step2:

Indexgruppe	Index
0/1	1,0 (1) * 4,0 (4) P1 8,0 (8) *
1/2	3,1 (2) * 9,1 (8) * 9,8 (1) *
2/3	7,3 (4) * 11,3 (8) * 11,9 (2) *
3/4	15,7 (8) * 15,11 (4) *

step3:

Indexgruppe	Index
0/1/2	9,8,1,0 (1,8) P2 9,1,8,0 (8,1)
1/2/3	11,9,3,1 (2,8) P3 11,3,9,1 (8,2)
2/3/4	15,11,7,3 (4,8) P4 15,7,11,3 (8,4)

P/M1	3	4	8	11
P1		*		
P2			*	
P3	*			*
P4	*			*

P1 = x3'x1'x0'
P2 = x2'x1'
P3 = x2'x0
P4 = x1x0

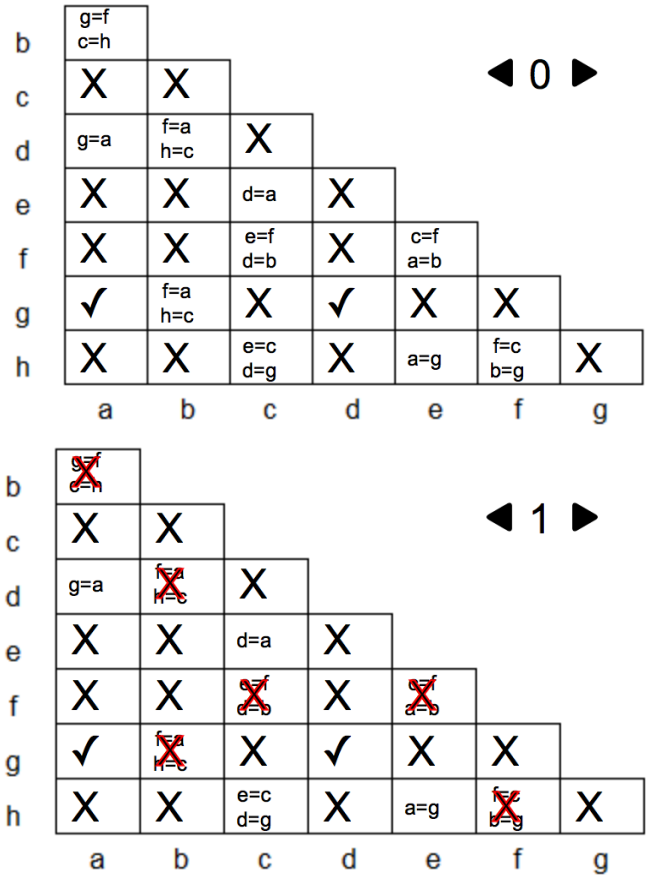
F = P1+P2+P3 = x3'x1'x0' + x2'x1' + x2'x0
or
F = P1+P2+P4 = x3'x1'x0' + x2'x1' + x1x0

Cost is 6.

Question 2: (8 points)
Minimize the states of the FSM described by the following state table using an implication table, then, redraw the state table:

Present State	Next State		Present Output
	X=0	X=1	
a	g	c	0
b	f	h	0
c	e	d	1
d	a	c	0
e	c	a	1
f	f	b	1
g	a	c	0
h	c	g	1

Answer:



The states that can be merged are:

a-g-d
e-c-h

Question 3: (16 points)

a) Draw the (gate-level) block diagram of a 4-bit ripple carry adder. (5 points)
b) Find the critical path of the adder and measure its delay considering that XOR gates have 2 ns delay and all other gates 1 ns delay (3 points)
c) Pipeline the adder so that each stage performs 1-bit addition (split the adder in 4 parts) and draw the block diagram. (5 points)
d) Measure the critical path of the pipelined adder considering that the flip-flops used have setup time T_{su}= 0.1 ns, propagation time T_p= 0.2 ns and hold time T_h= 0.1 ns. (3 points)

Answer:

a) Lecture 2 , ripple carry adder.
b) 10 ns
c) similar to the pipelined adder in lecture 18
d) 4.3 ns

Question 4: (8 points)
Draw the block diagram of a 4x2 memory block (4 elements, each being 2-bits wide). Consider each basic memory cell (that stores 1-bit) as a black box with 2 inputs (Data_in, Write_enable) and one output (Data_out).

Answer:
Similar to figure in lecture on arithmetic and memory slide 34 (only 2 bits wide instead of 3).

Question 5: (7 points)
Consider a design implemented both in ASIC and in FPGA technology. Which implementation would be better in terms of (i) power consumption, (ii) delay (performance), and (iii) silicon area, and why?

Answer:
Lecture on ASICs slide 26.
In short: ASICs are better in terms of power, delay and area. FPGAs have much more circuit to offer flexibility. Only a small fraction of this circuit is used in a particular design configuration.

Question 6: (14 points)

a) Draw the block diagram of an array multiplier (10 points)
b) Show its critical path (4 points)

(a full-adder can be used as a building block without showing its internals).

Answer:
Lecture on Arithmetic slide 18 (4-bit x 4-bit, if 3x3 array multiplier is drawn is also ok).

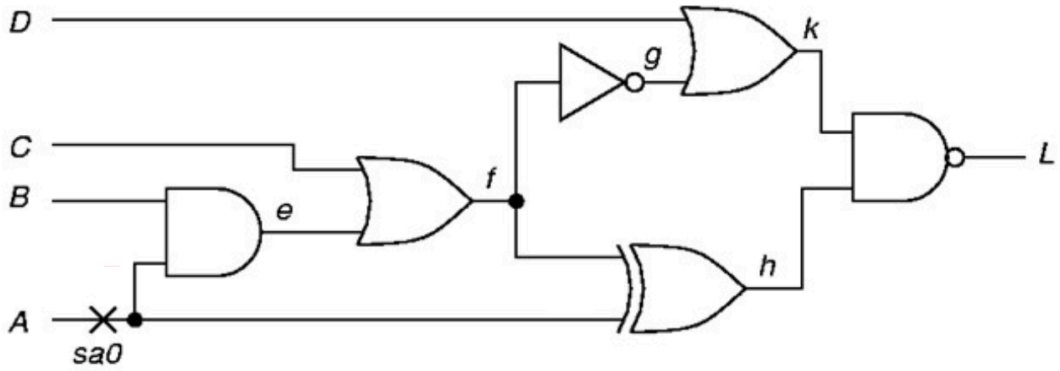
Question 7: (7 points)
The cost of a chip is 10 SEK when its yield is 60%. What will be its cost if the yield was increased to 90%?

Answer:
6.66667 SEK (similar to slide 32 of lecture on Testing)

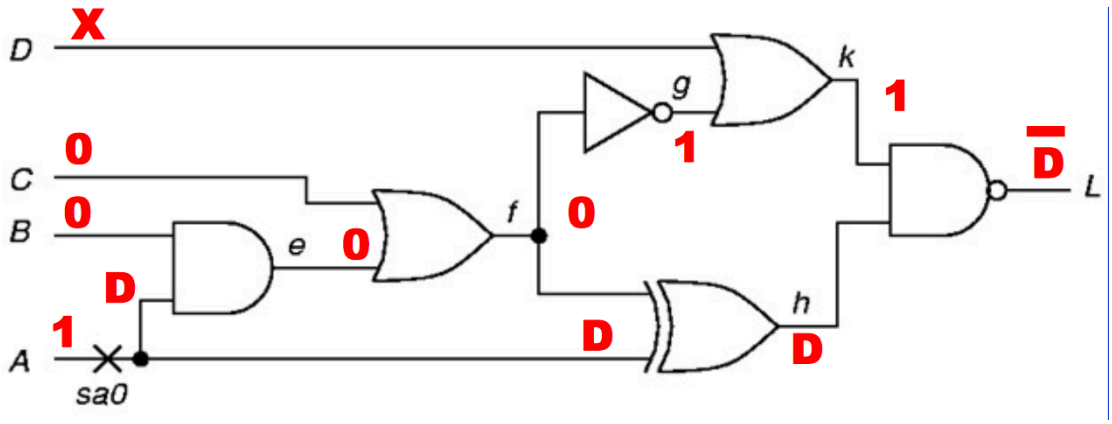
Question 8: (5 points)
What is the definition of clock skew?

Answer:
See respective slide in Lecture on Timing, Delay, Power.

Question 9: (10 points)
Find the test vector that activates and propagates a stuck-at-0 fault at input A.

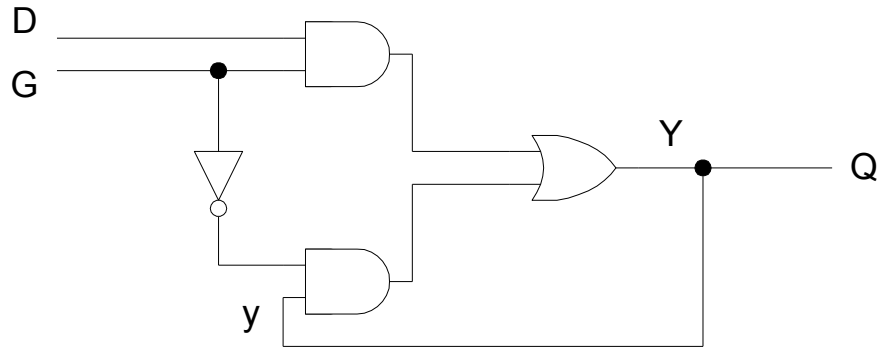


Answer:



Question 10: (15 points)

a) Starting from the following asynchronous circuit, make the necessary modifications to add a NOR-based SR-latch to the output. (9 points)
b) What are the advantages of the new design over the original one? (6 points)



Answer:
a) Similar to lecture on asynchronous (2nd half of the design example)
b) Latches protect against hazards. This design has a static-1 hazard (see same lecture-> hazards) which can be eliminated with a NOR based SR-latch.

END of EXAM