

EDA321/EDA322: Digital Design Exam - August 2016

Date: August 25, 2015

Time: **14:00-18:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries: Ioannis Sourdis (extension 1744); will visit the room at **15:30** and at **17:00**

Results and grading review: See me in my office 4110 on **September 19th at 10:00**.

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:

0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%

GU:

Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: Blank paper and a calculator are allowed. No textbooks or lecture notes, etc. allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Question 1: (10 points)

Minimize the cost of function $F(x_3, x_2, x_1, x_0) = \Sigma(1, 5, 14, 15) + D(0, 3, 7, 13)$ using Quine-McCluskey (x_0 is the list significant bit, x_3 is the most significant bit).

Measure the cost of the minimized function by counting the total number of 2-input gates of the circuit (inversions are not considered) e.g., $a*b + c*d$, has cost of 3.

Answer:

Truth table for the minterms $\Sigma(1, 5, 14, 15)$:

i	x3	x2	x1	x0	y
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	1

Truth table for the don't care terms $D(0, 3, 7, 13)$:

i	x3	x2	x1	x0	h*
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	0

The minterms and don't care terms are put together:

Step 1:

step2:

step3:

Indexgruppe	Index
0	0*
1	1*
2	3*
	5*
3	7*
	13*
	14*
4	15*

Indexgruppe	Index
0/1	1,0 (1) P1
1/2	3,1 (2) *
	5,1 (4) *
2/3	7,3 (4) *
	7,5 (2) *
	13,5 (8) *
3/4	15,7 (8) *
	15,13 (2) *
	15,14 (1) P2

Indexgruppe	Index
0/1/2	
1/2/3	7,5,3,1 (2,4) P3
	7,3,5,1 (4,2)
2/3/4	15,13,7,5 (2,8) P4
	15,7,13,5 (8,2)

P/M1	1	5	14	15
P1	*			
P2			*	*
P3	*	*		
P4		*		*

$$P1 = x3'x2'x1'$$

$$P2 = x3x2x1$$

$$P3 = x3'x0$$

$$P4 = x2x0$$

$$F = P2+P3 = x3x2x1 + x3'x0$$

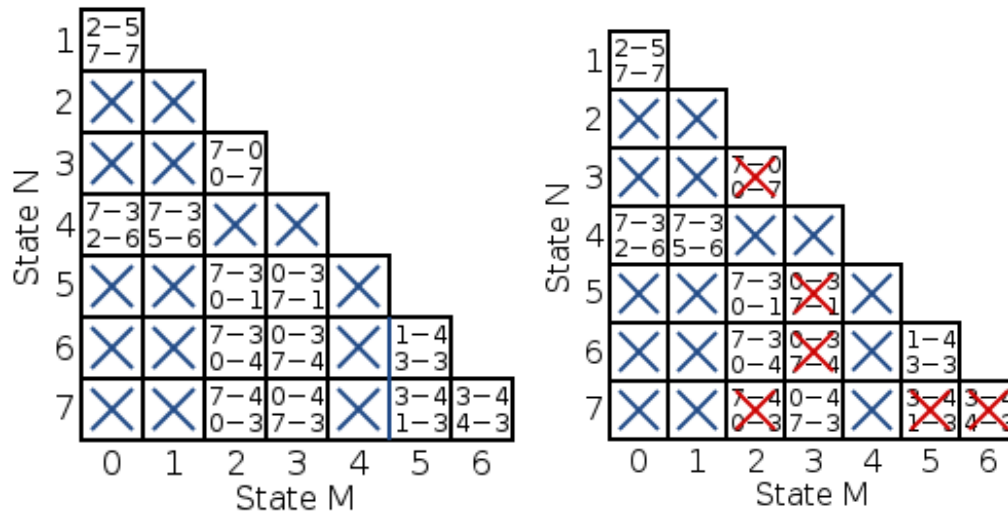
Cost is 4.

Question 2: (10 points)

Minimize the states of the FSM described by the following state table using an implication table, then, rewrite the state table:

Current State	Next State		Output	
	Input X		Input X	
	0	1	0	1
0	7	2	0	0
1	7	5	0	0
2	7	0	1	0
3	0	7	1	0
4	3	6	0	0
5	3	1	1	0
6	3	4	1	0
7	4	3	1	0

Answer:



Current State	Next State		Output	
	Input X		Input X	
	0	1	0	1
0	3	2	0	0
2	3	0	1	0
3	0	3	1	0

Question 3: (15 points)

- Write the logic functions that are used in an 8-bit carry-lookahead adder. (6 points)
- Draw the block diagram of an 8-bit carry lookahead adder. (6 points)
Note: use blocks that are described by the logic functions of (a) to avoid drawing the actual gates.
- Show the critical path (3 points)

Answer:

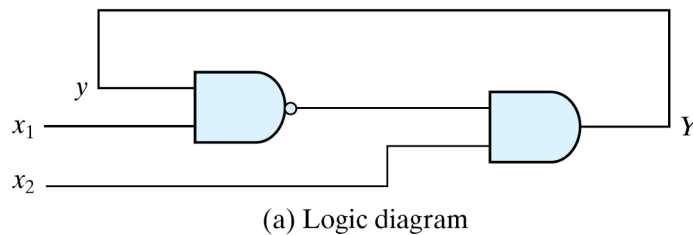
Lecture 2,

- slides 81, 85, 86,
- slide 87
- from $x_0, y_0 \rightarrow G_0, P_0 \rightarrow G_0^1, P_0^1 \rightarrow G_0^2, P_0^2 \rightarrow c_4 \rightarrow c_6 \rightarrow c_7 \rightarrow s_7$

Question 4: (12 points)

Analyze the following asynchronous circuit:

- Write its logic equations (3 points)
- Write the transition table, (3 points)
- Find the stable states. (2 points)
- What do you observe? (4 points)



Answer:

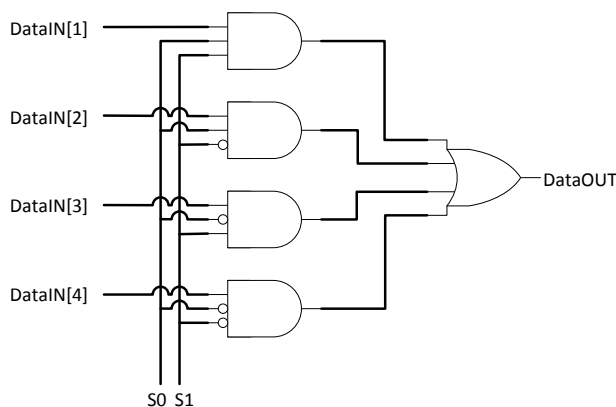
- a) $Y = (y * x_1)' * x_2$
- b) Lecture 17, slides 42
- c) Lecture 17, slides 42
- b) for $x_1 x_2 = 11$ the circuit is unstable since Y and y are not equal for neither for $y=0$ nor for $y=1$.

Question 5: (15 points)

- a) Draw the gate-level circuit of a 4-to-1 multiplexer (1 bit wide) with inputs: select (2-bits), DataIN (4-bits), DataOUT (1-bit) (1 points)
- b) What is the critical path of the design and how long is it (in ns) considering that 2-input gates have a delay of 1 ns, 3-input and 4-input gates have a delay of 2 ns, and inverters do not add any delay. (2 points)
- c) Pipeline the above design to reduce the critical path to $T \leq 2ns$. In other words, to make the design produce one result (one new output) every $T \leq 2ns$. Consider that a flip-flop has: (10 points)
 - a. propagation delay 100ps,
 - b. setup time 100ps
 - c. hold time 50ps
- d) What is the overall delay of the pipeline (the time for a set of inputs to produce a result)? (2 points)

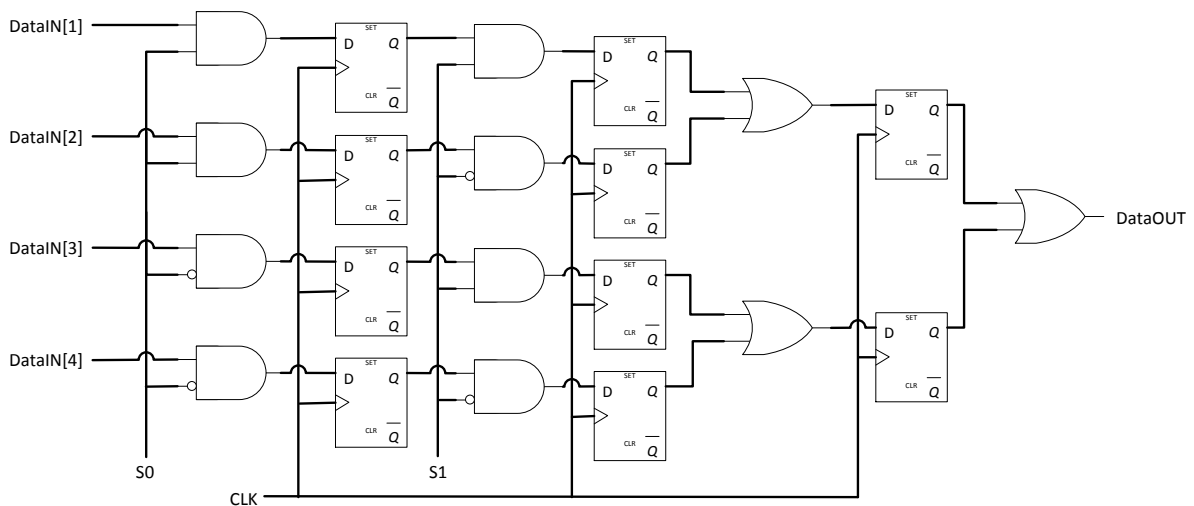
Answer:

a)



- b) From DataIN[1] or DataIN[2], DataIN[3], or DataIN[4] and S0, S1 to the DataOUT. That is 4 ns.
- c) Each stage has to have a depth of a single 2-input gate. If it has a 3- or 4-input gate the logic alone would have a delay of 2 ns and with the additional delay of the flip flop the critical path would be more than 2 ns.

Therefore, 4 stages are needed, one per 2 input gate



Then the critical path is $T = T_{prop} + Gate_Delay_{2input} + T_{setup} = 0.1 + 1 + 0.1 \text{ ns} = 1.2 \text{ ns}$

- d) The lowest clock period is 1.2 ns. A result needs 4 cycles to be created, therefore $4 * 1.2 \text{ ns} = 4.8 \text{ ns}$

Question 6: (6 points)

How does SRAM compare to DRAM in terms of (i) Density (and cell size), (ii) Cost per bit, (iii) Read latency, (iv) Technology process. (v) Give one example of use in a computing system for SRAM and one for DRAM. (vi) Which one of the two (SRAM and DRAM) requires refresh and why?

Answer:

- i) DRAM is denser as it has smaller cells
- ii) DRAM has lower cost per bit (mainly because it is denser)
- iii) DRAM read access is slower
- iv) SRAM is fabricated in the same CMOS technology as logic. DRAM requires different technology
- v) SRAM: register file, caches. DRAM main memory of a computer
- vi) DRAM requires refresh of the data frequently otherwise its contents are lost

Question 7: (10 points)

FPGAs can be reconfigured in order to implement different digital designs. Their logic cells can support various logic functions, and their reconfigurable interconnects can connect these logic cells in different ways.

- a) Show the block diagram of a logic cell (4-inputs) and explain how it can support any 4-to-1 (4-bit input, 1-bit output) logic function.
- b) Show how 4 logic cells can be interconnected with each other.

Answer:

Lecture 12

- a) slide 16
- b) slides 30, 31

Question 8: (12 points)

- a) Draw the block diagram of a 4-bit divider (6 points)
- b) Show step-by-step how the division $6/4$ would be performed in this divider (6 points)

Note: a 4-bit adder can be used as a building block without showing its internals.

Answer:

- a) Lecture 11, slide 24 (for 4-bits instead of 32)
- b) Lecture 11, slide 23

Question 9: (4 points)

The cost of a chip is 15 SEK when its yield is 80%. What will be its cost if the yield was increased to 95%?

Answer:

12.6 SEK

Question 10: (6 points)

Explain how a Flip-flop with asynchronous input can enter a metastable state? How can we reduce the probability of this (a flip-flop entering a metastable state) happening?

Answer:

Lecture 16, slides 31, 32, 33

END of EXAM