DAT480: Reconfigurable Computing
Exam - January 2022

Date: January 10, 2021

Time: **8:00-12:00**

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Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: Lecture notes are allowed.
Textbooks or Calculators are not allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

Note: *These are example answers to the exam questions for one possible set of randomized variables or explanations as of how a solution to an exam question can be derived.*

Question 1 Reconfigurable Devices: (12,5 points)
Consider the following Boolean function:

F(x1, x2, x3, x4)= A*x1 + B*x2*x3*x4 + C*x4

and map it to the following 3 FPGA devices:

- one with (i) 2-input LUTs,
- one with (ii) 3-input LUTs, and
- one with 4-input LUTs.

How many SRAM cells are used for implementing the function in each case?

Answer

Similar to lecture on Reconfigurable Devices, slide 20

Question 2 Compute Models: (12,5 points)
Describe the main differences between a Dataflow and a Sequential Control flow Compute Model. Which one fits best Reconfigurable Computing and why?

Answer
See lecture on Reconfigurable System Architectures, slides about "Basic Concepts of Computing in Space".

Question 3 Reconfigurable System Architectures: (12,5 points)
Describe how you can extend an existing Instruction Set with a handful of instructions to support a reconfigurable functional unit, while avoiding the risk of opcode space explosion.

Answer
See lecture on Reconfigurable System Architectures, Molen Architecture / Instruction Set Extension

Question 4 Application Development in Reconfigurable hardware: (12,5 points)
Describe three application characteristics which indicate that performance acceleration can be achieved if the application is implemented in reconfigurable hardware. Explain why reconfigurable hardware is a good fit in each case.

Answer
See lecture on Application Development in Reconfigurable hardware, slide 5-7

Question 5 Software for Spatial computing: (12,5 points)

Consider the following code:

```
for i=1 to N
  in = stream_in[i];
  for j=1 to M {
     in = in*in*in;
  }
stream_out[i] = in;
```

Consider also F(x) is pipelined in 2 stages (2 cycles, each spend for one multiplication) and a single multiplication requires area Z.

How much area do you need in order for your spatial computing implementation of the code to achieve processing throughput of one input element (stream_in[i]) per cycle? Show the block diagram of this hardware implementation.

Consider now that the total available area for implementing the computations of the code is Z. Show the block diagram of this hardware implementation and calculate it's throughput.

Answer

Similar to lecture on HLS programming and HW/SW co-design, examples in slides 38, 44

- You'd need 2*M*Z area for processing a new input every cycle (similar to slide 38 – fully unrolled loop)
- With Z area, M*2 iteration need to be performed on the same hardware for each input, so the throughput is 1 input per M*2 cycles (similar to slide 44)

Question 6 Reconfiguration Management: (12,5 points)

What is a multi-context FPGA and what are the advantages and disadvantages compared to a single-context FPGA.

Answer

See lecture on reconfigurable management, slides 9, 11.

Briefly, Multi-context FPGAs allow fast switching between configurations, avoiding the configuration latency. They "pay" this flexibility with extra hardware to store and switch between configurations.

Question 7 Energy Efficiency: (12,5 points)

Describe the concept of Guarded evaluation and how it can be used to reduce switching activity and power consumption. Can you find similarities and differences with Clock gating?

Answer
See lecture on Energy efficiency, slide 39 and 48.
Briefly, in guarded evaluation hidden latches prevent switching of operands to functional units that are not used. In clock gating, a clock enable signal is generated only when a set of registers/flip-flops are updated (written), otherwise the clock is disabled, preventing it from switching at every flip-flop.

In both cases the circuit is enabled only when used. Guarded execution is focused on Functional units (or any other Boolean logic), while clock gating is focused on the clock provided to flip-flops.

Question 8 Defect and Fault Tolerance: (12,5 points)

a) What is the definition of yield in the fabrication process of a chip?
b) How is the yield affected with the (i) size of the chip, (ii) size of substitutable units in the chip? Justify your answer.

Answer
See lecture on defect and fault tolerance, slide 5, 7, 10