Exam, Mixed-Signal System Design (DAT116)

January 12, 2018

Time and place: Friday January 12, 8:30–12:30, room EF

Examiner: Lars Svensson, Lena Peterson

Department: Computer Science and Engineering

Solutions: Will be posted on the course homepage on Jan 15

Results: Will be posted in LADOK on or before February 2

Grading review: Time and place to be posted on the course homepage

Grade limits:

U: 0–29 points; 3: 30–39 points; 4: 40–49 points; 5: 50– points

Bonus points from 2017 version of omnibus report will be added to the score before computing the final grade.

Allowable references and utilities: Open-book exam. Text books, lecture notes, research article printouts, and lab reports are admissible. Errata sheet printout for textbooks are also OK, as is a calculator.

General: Submit your solutions, ***in English***, on blank papers sheets. Write legibly; feel free to use figures to get your point across.

Please start the solution for each problem on a new sheet. Please number the sheets so that solutions are in numerical order.

In some problems, it may be necessary to make assumptions or to introduce variables etc. When you do, state your assumptions explicitly and motivate them. Reasoning and descriptions may give partial credit even if the end result is not 100% correct.

Please note that your personal identity code is required on each submitted sheet!

Good luck!

Problems

Each sub-problem is worth five points, for a total of 60 points.

You may need the value of Bolzmann's constant: $k = 1.38 \times 10^{-23}$ J/K. These trigonometrical identities may also come in handy:

$$\sin 2\alpha = 2 \sin \alpha \cos \alpha$$

$$\cos 2\alpha = \cos^2 \alpha - \sin^2 \alpha$$

$$\sin 3\alpha = 3 \sin \alpha - 4 \sin^3 \alpha$$

$$\cos 3\alpha = 4 \cos^3 \alpha - 3 \cos \alpha$$

$$\sin 4\alpha = 4 \sin \alpha \cos \alpha - 8 \sin^3 \alpha \cos \alpha$$

$$\cos 4\alpha = 8 \cos^4 \alpha - 8 \cos^2 \alpha + 1$$

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1. A single-sinewave signal of varying amplitude and a frequency less than 10 MHz is to be sampled and converted to digital form. The peak-SNR requirement is 72 dB.

   (a) Suggest minimum values of sample frequency and quantizer resolution to fulfill the specification.

   (b) The same setup, with parameters as per task 1a, is used to convert a signal $x(t)$ composed of two equal-amplitude sine waves:

   $$x(t) = A(sin(2\pi f_1 t) + sin(2\pi f_2 t))$$

   f_1 and f_2 are both less than 10 MHz but are *not* rationally related. Estimate the resulting peak SNR.

   (c) Suggest and motivate sample-clock jitter requirements for the two conversion situations above.

2. Emilia needs to A/D-convert a baseband signal with a bandwidth of 500 kHz. An unused 4-bit quantizer is available in the system she works on; but she needs to apply noise shaping to improve the SNDR.

   (a) Aware that noise-shaping feedback loops may misbehave at high input power levels, Emilia decides to limit her input signal to 3 dB below full scale. What peak SNDR should she expect for a first-order loop filter, a sample rate of 16 MHz, and appropriate digital filters to remove the out-of-band noise?

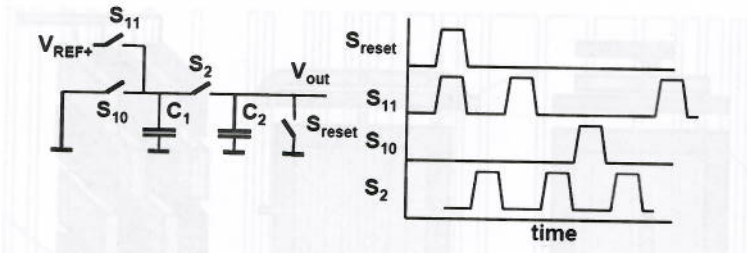
   (b) To suppress spurious tones at low DC inputs, Emilia decides to try adding some white dither noise to the input signal. What noise power might she apply without destroying the SNDR at higher input power levels? Note: you need to specify the noise bandwidth.

   (c) Emilia fears that her feedback DAC might suffer from a third-order nonlinearity:

   $$y = x - \alpha x^3$$

   If the full range of the input signal is ± 1, what is the maximum acceptable value of α? Motivate.

3. The figure below (from Pelgrom: Analog-to-Digital conversion, Springer 2010) shows a very simple D-to-A converter, and timing diagrams for the operation of the switches.



Bits (b_i) are processed in sequence, from the least to the most significant bit, and activate the switches S_{11} and S_{10} for values 1 and 0, respectively. After each step, the output voltage is given by:

$$V_{out}(i) = \frac{C_1}{C_1 + C_2} b_i V_{REF+} + \frac{C_2}{C_1 + C_2} V_{out}(i-1)$$

The analog result appears at V_{out} after N cycles.

(a) Derive the output voltage as a function of the input bits under the assumption that $C_1 = C_2$.

(b) Identical capacitors can be closely matched (at an area cost). Estimate the ENOB value possible with a converter like this if C_1 and C_2 can be matched to within 0.1%.

(c) The converter is operated at a rate of 10^6 complete conversions per second, with a resolution corresponding to the ENOB you calculated in the previous task (please assume an ENOB value if you did not solve the previous task). Assume that V_{REF+} is 2 V. How large must each capacitor be for the kT/C noise to be insignificant when compared with the matching error?

4. Medical implants such as heart pacemakers have stringent low-power requirements, both to maximize battery life and to minimize heating of surrounding tissues. A recent PhD thesis[1] describes an 8-bit, 11 kS/s ADC with a power dissipation of 2.83μW. The INL is quoted as ≈ 1 LSB, and the SNDR as 47 dB for a 1-kHz signal 0.2 dB below full scale.

(a) The quoted power dissipation is very low; but speed and resolution requirements are not very challenging. How does this design compare to the state-of-the-art in low-power converters?

(b) With the simplifying assumption that the INL is due to a second-order nonlinearity, calculate the input-related IP2 for the converter.

(c) What limits the peak SNDR of the converter: the quantization error, the nonlinearity, or something else?

THE END

[1] Song Jinxin. *Ultra low power Analog-to-Digital Converter for Biomedical Devices.* PhD Thesis, Royal Institute of Technology, Stockholm, March 2011.