

Exam, Mixed-Signal System Design (DAT116)

January 13, 2017

Time and place: Friday January 17, 14:00 – 18:00, M-building

Examiner: Lars Svensson, Lena Peterson

Department: Computer Science and Engineering

Inquiries: Lars Svensson (extension 1704); will visit the room at 15:00 and at 17:00

Solutions: Will be posted on the course homepage on Jan 16

Results: Will be posted in LADOK on or before February 3

Grading review: Time and place to be posted on the course homepage

Grade limits:

U: 0–29 points; 3: 30–39 points; 4: 40–49 points; 5: 50– points

Bonus points from 2016 version of omnibus report will be added to the score before computing the final grade.

Allowable references and utilities: Open-book exam. Text books, lecture notes, research article printouts, and lab reports are admissible. Errata sheet printout for textbooks are also OK, as is a calculator.

General: Submit your solutions, *in English*, on blank papers sheets. Write legibly; feel free to use figures to get your point across.

Please start the solution for each problem on a new sheet. Please number the sheets so that solutions are in numerical order.

In some problems, it may be necessary to make assumptions or to introduce variables etc. When you do, state your assumptions explicitly and motivate them. Reasoning and descriptions may give partial credit even if the end result is not 100% correct.

Please note that your personal identity code is required on each submitted sheet!

Good luck!

Problems

Each sub-problem is worth five points, for a total of 60 points.

You may need the value of Boltzmann's constant: $k = 1.38 \times 10^{-23}$ J/K. These trigonometrical identities may also come in handy:

$$\sin 2\alpha = 2 \sin \alpha \cos \alpha$$

$$\cos 2\alpha = \cos^2 \alpha - \sin^2 \alpha$$

$$\sin 3\alpha = 3 \sin \alpha - 4 \sin^3 \alpha$$

$$\cos 3\alpha = 4 \cos^3 \alpha - 3 \cos \alpha$$

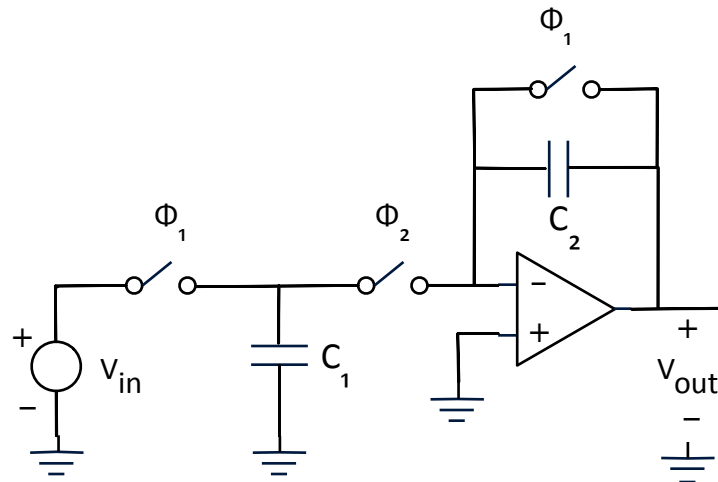
$$\sin 4\alpha = 4 \sin \alpha \cos \alpha - 8 \sin^3 \alpha \cos \alpha$$

$$\cos 4\alpha = 8 \cos^4 \alpha - 8 \cos^2 \alpha + 1$$

1. A low-pass signal with a bandwidth of 5 MHz is to be sampled and converted to digital form. The overall peak-SNR requirement is 54 dB.
 - (a) Suggest minimum values of clock frequency and quantizer resolution to fulfill the specifications.
 - (b) Outside the band of interest, uninteresting and potentially destructive signals (i.e. noise) can occur at the same power levels as those in the band of interest. How will you select the sample rate if you can afford a pre-sampling anti-alias filter of at most order 3? Motivate.
 - (c) To save production cost, a junior designer who has not passed DAT116 replaces the pre-sampling filter with a cheaper second-order version. What happens to the worst-case peak SNR?

2. Noise-shaping A/D converters make it possible to reach high SNR figures despite modest component precision. However, the overall SNR may still be limited by the linearity of the feedback-loop DAC.
 - (a) Estimate the necessary OSR for a first-order low-pass sigma-delta loop with a three-bit quantizer and a perfectly linear three-bit feedback DAC, when the overall SNR requirement is 69 dB.
 - (b) Next, assume that the DAC has a second-order nonlinearity with a maximum INL of 2% of the full range. Estimate the reachable SNR for a full-range low-frequency signal. Motivate.
 - (c) The situation may be improved with the introduction of dynamic element matching in the feedback DAC. Estimate the possible improvement. Motivate.

3. The switched-capacitor amplifier in the figure below is included in the signal path in a data conversion system.



During Φ_1 , the input voltage V_{in} is sampled onto capacitor C_1 , and the feedback capacitor C_2 is reset. During Φ_2 , the input is disconnected and the charge on C_1 is moved to C_2 , such that the output voltage is $V_{out} = -(C_1/C_2)V_{in}$. The desired gain magnitude of the amplifier is 2. You may assume that the capacitors are perfectly matched.

The opamp has a raw gain which in itself is large enough not to limit your performance. However, it is maximally capable to source or sink an output current of $1\mu\text{A}$, regardless of the output voltage, which can range from 0V to 1.2V (that is, across the entire supply voltage range; as is customary, the ground signs in the figure correspond to the midpoint of the supply range).

- Capacitances occupy expensive chip area and are therefore targets for minimization. What minimum total capacitance ($C_1 + C_2$) is needed to support an ENOB of 12 bits?
 - Estimate the maximum clock frequency possible with capacitances as in task 3a.
 - If you additionally know that the output resistance of the opamp is $65\text{k}\Omega$, how does this information affect your estimate of the maximum clock frequency?
4. During the course, you have learned about time interleaving as a technique to improve the performance of ADCs. In a recent publication¹, the authors describe a technique which uses two-way time interleaving to improve the performance of a DAC. (Two identical sub-DACs are connected to a multiplexer which connects one of the sub-DAC outputs to a dummy load while the other sub-DAC output is being used, and then swaps the two sub-DACs for the next sample. Thus, the two sub-DACs convert alternate samples. The benefit is that any value-dependent, and thus non-linear, output glitching can take place while the sub-DAC is connected to the dummy load, so the distortion never reaches the actual output.)
- Many of the important performance parameters for the DAC are given already in the publication title. Estimate the timing accuracy requirement for the multiplexer control signal.

¹Erik Olieman et al. A 110mW , 0.04mm^2 , 11GS/s 9-bit interleaved DAC in 28nm FDSOI with $>50\text{dB}$ SFDR across Nyquist. *Proceedings of the IEEE Symposium on VLSI*, 2014.

- (b) Illustrations in the article show that the worst spurious signal corresponds to the third harmonic of the input signal at an input frequency of 4.6 GHz. At what frequency does this spurious signal appear in a full-bandwidth spectrum plot?
- (c) How does the power dissipation of this DAC compare with that expected for an ADC with similar performance? Motivate your answer.

THE END