Solutions to Jan 13 exam
Mixed-Signal Systems (DAT116)

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The following are suggested solutions to the problems. It must be noted that other solutions may be possible, and that approximate solutions will give at least partial credit as long as the approximations are reasonable (just as in real life!).

1. (a) According to Nyquist, a baseband signal with a bandwidth of 5 MHz needs to be sampled with at least 10 MHz. The 54-dB SNR requirement translates to an ENOB value of $(54 - 1.76)/6.02 = 8.68$, so at least 9 bits would be necessary.

   (b) The filter passband edge should be at 5 MHz to let the band of interest through unscathed; the lowest mirror frequency of the passband edge should be suppressed by at least 54dB. The rolloff of a third-order filter is 18 dB per octave, so 54 dB corresponds to 3 octaves, which is a factor of 8. Then the sample rate must be at least 9 times f_B, that is 45 MHz. [You may feel that this is surprisingly high compared to what Nyquist requires! This is due to the unusually high noise level. In a case like this, it might be worthwhile to investigate a filter with zeroes in the stopband.]

   (c) The 3 octaves now each contributes 12 dB of attenuation rather than 18, so $3 \times (18 - 12) = 18$dB of attenuation is missing at the edge of the passband mirror. This SNR loss corresponds to a loss of 3 bits of resolution.

2. (a) A three-bit quantizer provides $6.02 \cdot 3 + 1.76 = 19.8$dB of base SNR. With an overall requirement of 69dB, $69 - 19.8 = 49.2$dB have to come from oversampling. A first-order loop contributes 9dB per octave (minus a constant penalty of 5dB), so six octaves (a factor of $2^6 = 64$) should just suffice.

   (b) Any feedback DAC nonlinearity will appear as if it were applied directly to the input signal. A second-order non-linearity with a maximum INL of 2% will add a second-order distortion power on the order of $0.02^2 \approx 0.0004$, that is, on the order of 34 dB below the power of a full-scale signal. If the input signal frequency is low enough, the full distortion power is still in the band of interest and will therefore be unaffected by the filters that remove the shaped noise. Thus, we can expect the distortion to limit the overall converter SNR.

   (c) The error power is now spread out across the entire frequency range. With an OSR of 64, only 1/64 of the power should now affect the output signal. In other words, the distortion should be suppressed by $3 \cdot 6 = 18$dB. We may hope for a total SNDR of of $34 + 18 = 52$dB, which is still worse than the 69dB in the specification.

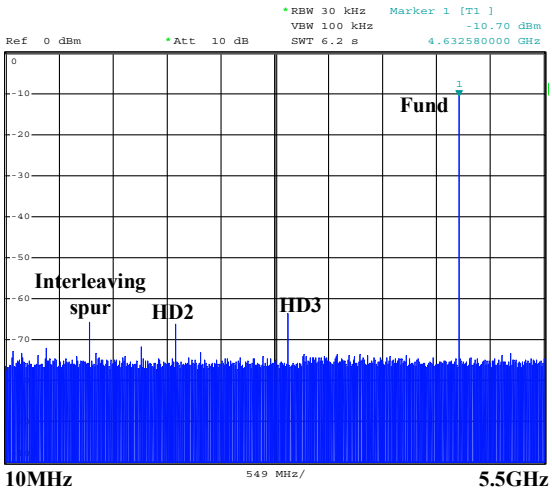
3. (a) Since $C_1/C_2 = 2$, C_2 is the smallest capacitance that is separately switched, and it therefore contributes the highest kT/C noise. With a full-scale voltage of 1.2V, $C_2 > 12kT \cdot 2^{2\cdot 12}/1.2^2 = 0.58$pF. The total capacitance is then $3 \times C_2 = 1.74$pF.

   (b) The opamp has to be able to charge C_2 from 0 to ± 0.6V (or conversely) during one phase, which will take $t = Q/I = CV/I = (0.58\text{p} \cdot 0.6)/1\mu = 0.35\mu$s. One full cycle is two phases, so the clock frequency can be at most 1.44MHz.

   (c) An output resistance of 65kΩ will result in a time constant of $65\text{k} \cdot 0.58\text{p} = 38$ns. To support 12 bits of precision, the circuit needs to settle to 1 part in $2^{12} \approx 4000$; the time t this takes may be found from $e^{-(t/RC)} = 1/4000$; then, $t \approx 9RC = 0.34\mu$s. This is roughly the same time as would be needed for constant-current settling (according to task 3b above); but in a pure RC charging, the initial current would be $0.6/65\text{k} = 9.2\mu$A, which the opamp is incapable of delivering. Thus, constant-current charging will continue until the output voltage is reduced by a factor of 9.2, i.e., to 11% of the original voltage, which will take 89% of 0.35μs, or 0.32μs. Then, RC settling will take over and run until 1 part in $9.2/4000 \approx 0.0023$, which takes $-\ln 0.0023 \approx 6$ time constants, or $6 \cdot 38 = 228$ns. The total time needed is then $0.32 + 0.23 = 0.55\mu$s, corresponding to a clock frequency of 910kHz.

4. (a) Timing inaccuracy is another term for sample jitter. At 11GS/s, the highest signal frequency is 5.5GHz. The paper title does not specify the ENOB of the converter; but 9 bits is enough to support 56 dB. Then, Maloberti's formula 1.8 indicates that $\Delta t_{RMS} = 10^{(-56/20)}/(2\pi \cdot 5.5\text{G}) = 46$fs will be tolerable at the worst-case (maximum) signal frequency.

   (b) The third harmonic of a 4.6-GHz signal would be at 13.8 GHz. This frequency is folded at 5.5 GHz and again at 11 GHz to appear at 2.7 GHz. The figure below (taken from the publication) shows the harmonic marked with "HD3".



   (c) The room-temperature ADC sample power at 11 GHz and 9 bits is $P_S = 12kTf_S 2^{2N} = 0.143$mW. The quoted dissipation (110mW) is 768 times larger than this power, so somewhat higher than what might be expected from the very most power-frugal ADC designs (but still within the overall range of what is being published now).