Exam, Mixed-Signal System Design (DAT116)

April 18, 2015

Time and place: Saturday April 18, 8:30 – 12:30, V building

Examiner: Lars Svensson, Lena Peterson

Department: Computer Science and Engineering

Inquiries: Lars Svensson (extension 1704); will visit the room at 9:30 and at 11:30

Solutions: Will be posted on the course homepage on April 20

Results: Will be posted in LADOK on or before May 3, 2015

Grading review: May 6, 2015; time and place to be posted on the course homepage

Grade limits:

U: 0–29 points; 3: 30–39 points; 4: 40–49 points; 5: 50– points

Bonus points from omnibus report will be added to the score before computing the final grade.

Allowable references and utilities: Open-book exam. Text books, lecture notes, research article printouts, and lab reports are admissible. Errata sheet printout for textbooks are also OK, as is a calculator.

General: Submit your solutions, ***in English***, on blank papers sheets. Write legibly; feel free to use figures to get your point across.

Please start the solution for each problem on a new sheet. Please number the sheets so that solutions are in numerical order.

In some problems, it may be necessary to make assumptions or to introduce variables etc. When you do, state your assumptions explicitly and motivate them. Reasoning and descriptions may give partial credit even if the end result is not 100% correct.

Please note that your personal identity code is required on each submitted sheet!

Good luck!

Problems

Each sub-problem is worth five points, for a total of 60 points. You may need the value of Bolzmann's constant: $k = 1.38 \times 10^{-23}$ J/K. These trigonometrical identities may also come in handy:

$$\sin 2\alpha = 2 \sin \alpha \cos \alpha$$

$$\cos 2\alpha = \cos^2 \alpha - \sin^2 \alpha$$

$$\sin 3\alpha = 3 \sin \alpha - 4 \sin^3 \alpha$$

$$\cos 3\alpha = 4 \cos^3 \alpha - 3 \cos \alpha$$

$$\sin 4\alpha = 4 \sin \alpha \cos \alpha - 8 \sin^3 \alpha \cos \alpha$$

$$\cos 4\alpha = 8 \cos^4 \alpha - 8 \cos^2 \alpha + 1$$

1. A certain embedded system needs to acquire a baseband signal with a bandwidth $f_B = 7$MHz.

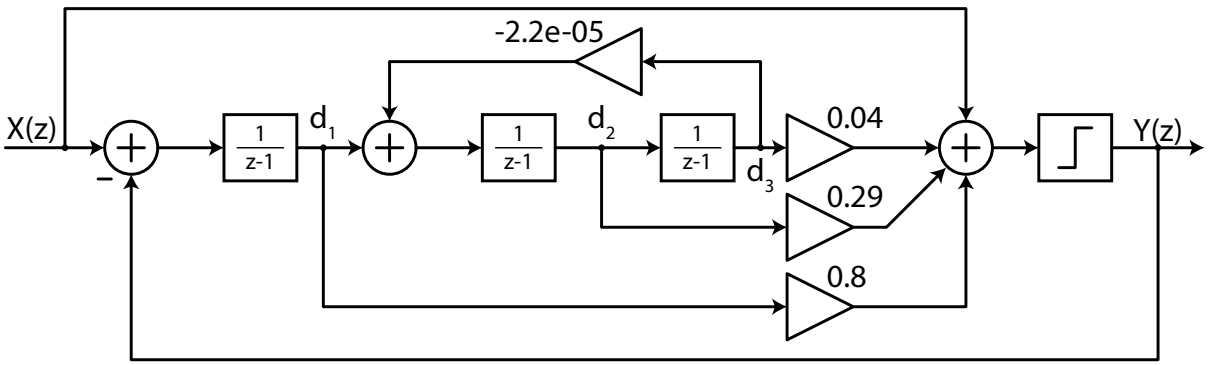
   (a) Two possible clock signals are available:
   - One high-quality clock at 21MHz
   - One 35-MHz clock which has a significant random jitter ($\Delta t_{RMS} = 100$ps)

   Which clock signal will allow the best overall SNDR with a third-order anti-aliasing filter? Assume that out-of-band signals may have one hundredth of the power of the desired in-band signals before filtering.

   (b) Suggest a suitable converter resolution for the acquisition task described above.

   (c) Estimate the theoretical power-dissipation limit for the converter you have just specified.

2. The figure below shows a one-bit $\Delta\Sigma$ modulator used as a design example in a recent publication[1]. **NOTE:** In the following, you may disregard the small feedback term $-2.2 \cdot 10^{-5}$.



   (a) What is the signal transfer function of this modulator?

   (b) What is the noise transfer function of this modulator?

   (c) Estimate the OSR necessary to reach a peak SNDR of 50 dB with this modulator.

[1] J. Johansson, L. Svensson. *A novel speculative pseudo-parallel* $\Delta\Sigma$ *modulator.* NORCHIP 2014, Tampere, Finland, Oct 27–28, 2014.

3. A certain analog processing element suffers from a third-order nonlinearity, that is, the instantaneous value of the output signal y for an input signal x is given by:

$$y(t) = x(t) - \alpha(x(t))^3$$

where α determines the severity of the nonlinearity.

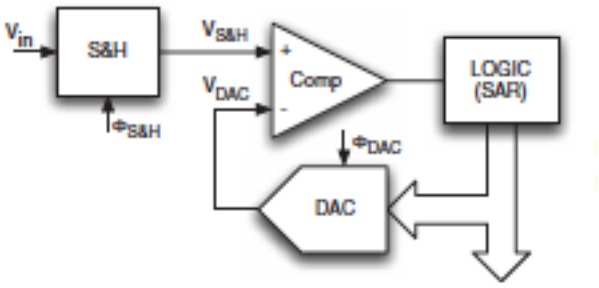
   (a) The compression point may be defined as the input level at which the output level at the fundamental frequency is 1 dB lower than the linear small-signal behavior would suggest. Derive the compression point for the nonlinear element as a function of α.

   (b) For $\alpha = 0.1$, express the compression point in dB related to a single sine wave with the amplitude 1.

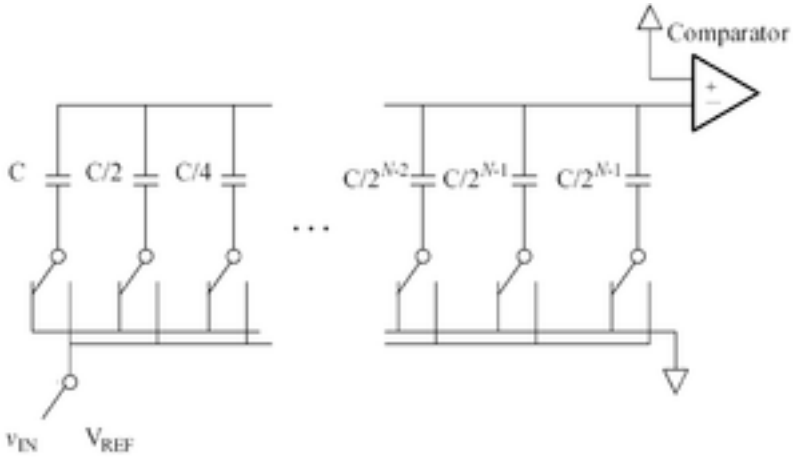
   (c) Derive the third-order intercept point for the element, in dB related to the compression point. Again use $\alpha = 0.1$.

4. In a 2014 ISSCC paper[2], Lukas Kull and coworkers present an 8-bit A-to-D converter with the conversion rate of 90 GS/s. This impressive performance level is reached by operating 64 identical successive-approximation (SAR) converters in a time-interleaving fashion. This problem focuses on the DAC included in each SAR converter.

   The basic operation of the Kull SAR converter corresponds to this picture from Maloberti:

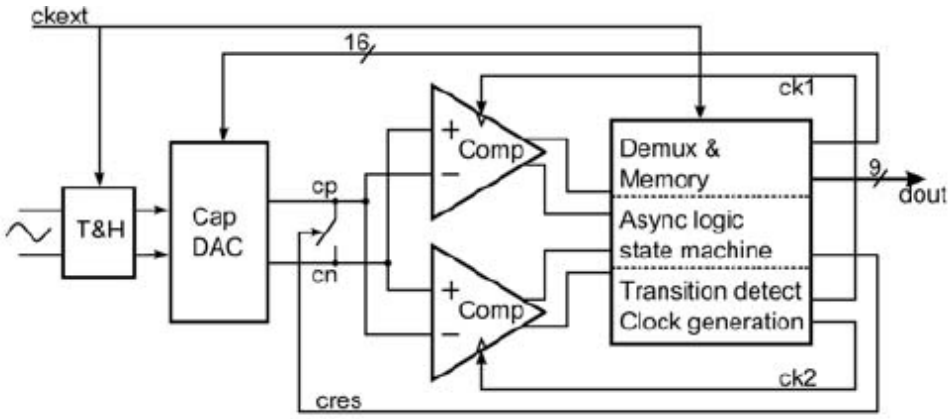


   The DAC is similar to this conceptual schematic:



[2] L. Kull et al. *A 90GS/s 8b 667mW 64x Interleaved SAR ADC in 32nm Digital SOI CMOS.* ISSCC 2014, pp. 378–379.

As is to be expected from an extreme-performance design, the practical implementation is considerably more involved. First, the DAC output is initiated with the sampled analog value, and the iterations of the SAR loop aim to reset the value to zero. Second, all analog signals are dual-rail, for speed and robustness. Also, two comparators are used alternately to allow one to recover while the other one operates. This picture is taken from an earlier paper[3] by the same authors:



Some other pertinent facts are as follows:

- Nominal full-scale input range: 500mV_{pp}
- Supply voltage range: 0.8 – 1.2 V (nominal value: 1 V)
- Operating temperature: up to 100°
- Silicon process: 32-nm SOI
- Chip area: 470×960 μm

(a) According to still another earlier paper[4] by the same authors, the ENOB of the complete ADC is mainly limited by thermal noise. Estimate the minimum value of C in the conceptual DAC schematic on page 3 for an ENOB of 8 bits.

(b) In the actual implementation, the minimum capacitor is limited to 2 fF due to matching concerns. Furthermore, for each of the two signal rails, the capacitor array is duplicated with a positive and a negative reference voltage, respectively. Estimate the energy required for one full conversion, assuming that each capacitor is completely charged and discharged once.

(c) In order to reduce the energy per operation and the DAC input capacitance, Kull scales the reference voltages of the two least-significant bits so that the three least-significant-bit capacitors can all be minimum-sized. Estimate the energy needed for one conversion after this optimization has been applied, with the same conditions as in the previous task. Can you think of another benefit from this refinement?

THE END

[3] L. Kull et al. *A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS.* ISSCC 2013, pp. 468–469.

[4] L. Kull et al. *A 35mW 8b 8.8GS/s SAR ADC with Low-Power Capacitive Reference Buffers in 32 nm Digital SOI CMOS.* ISVLSI '13.